Enlightenment Beyond Classical CMOS

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Director Technology Strategy

Intel Fellow

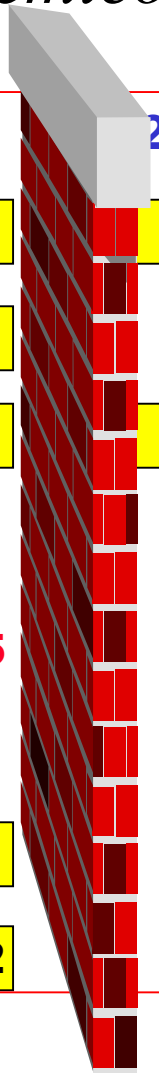

Who is afraid of
"The Red Brick Wall???"

Approaching a "Red Brick Wall"

1999 Results

Challenges/Opportunities for Semiconductor R&D

Year of Production:	1999	2002	2005	2008	2011	2014
DRAM Half-Pitch [nm]:	180	130	100	70	50	35
Overlay Accuracy [nm]:	65	45	35	25	20	15
MPU Gate Length [nm]:	140	85-90	65	45	30-32	20-22
CD Control [nm]:	14	9	6	4	3	2
T_{OX} (equivalent) [nm]:	1.9-2.5	1.5-1.9	1.0-1.5	0.8-1.2	0.6-0.8	0.5-0.6
Junction Depth [nm]:	42-70	25-43	20-33	16-26	11-19	8-13
Metal Cladding [nm]:	17	13	10	0	0	0
Inter-Metal Dielectric K:	3.5-4.0	2.7-3.5	1.6-2.2	1.5	<1.5	<1.5

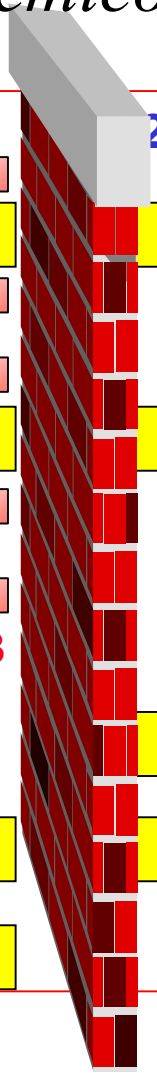


Moving Closer to the "Red Brick Wall"

2001 Results

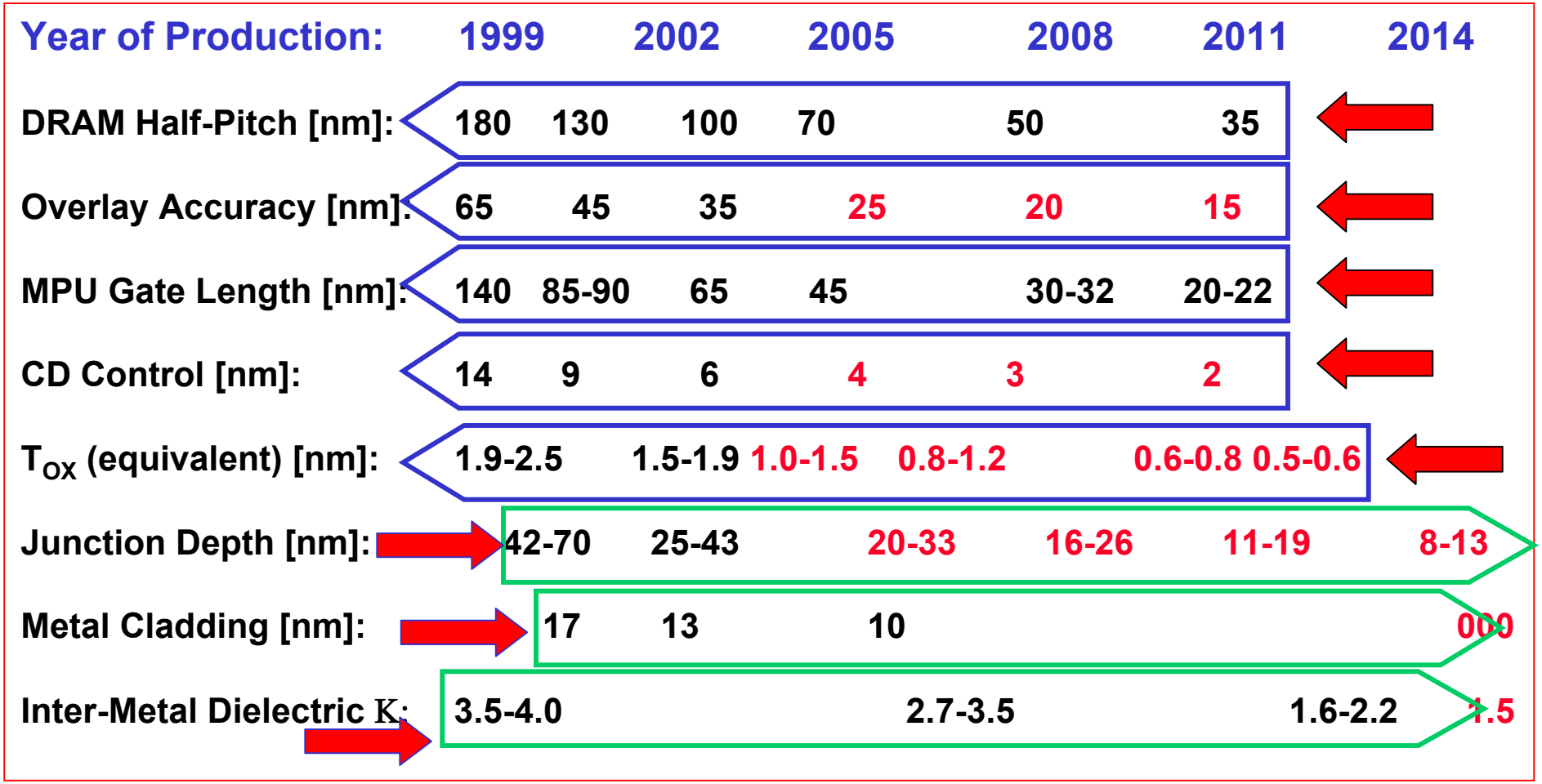
Challenges/Opportunities for Semiconductor R&D

Year of Production:	2001	2003	2005	2007	2010	2016
DRAM Half-Pitch [nm]:	130	100	80	65	45	22
Overlay Accuracy [nm]:	46	35	28	23	18	9
MPU Gate Length [nm]:	90	65	45	35	25	13
CD Control [nm]:	8	5.5	3.9	3.1	2.2	1.1
T_{OX} (equivalent) [nm]:	1.3-1.6	1.1-1.6	0.8-1.3	0.6-1.1	0.5-0.8	0.4-0.5
Junction Depth [nm]:	48-95	33-66	24-47	18-37	13-26	7-13
Metal Cladding [nm]:	16	12	9	7	5	2.5
Inter-Metal Dielectric K:	3.0-3.6	3.0-3.6	2.6-3.1	2.3-2.7	2.1	1.8



Roadmap Acceleration and Deceleration

2001 versus 1999 Results



Three Step Strategy on How to Crash the Red Brick Wall

1. Demonstrate transistor functionality using classical CMOS process down to:
    1. Lg=30nm, December 2000
    2. Lg=20nm, June 2001
    3. Lg=15nm, November 2001
2. Identify solutions for each of the classical CMOS limitations (2001/2002)
3. Engineer each of the new technology building blocks with material and equipment suppliers (2002/2004)

Agenda

- ***Solid State Physics Refresher***
- MOS Device Physics Refresher
- Classical CMOS Limitations
- Non-classical CMOS
- New Emerging Technologies
- Conclusions

Energy of a Particle in Free Space

$F=ma$

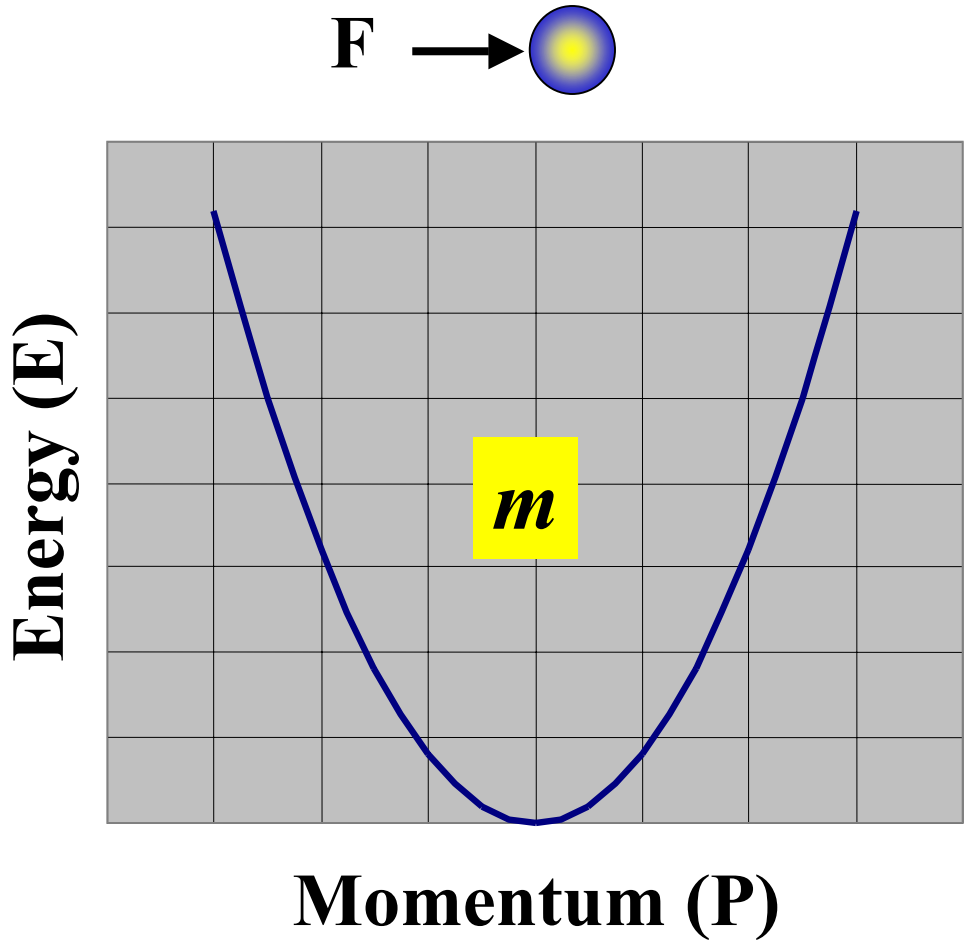
$v=at$

$p=mv$

$E=(1/2)mv^2$

$E=p^2/2m$

$$m = \frac{1}{\delta^2 E/\delta p^2}$$



Effect of Mass on Particle Energy

$F=ma$

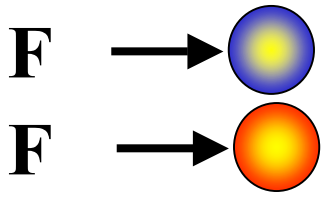
$v=at$ $\quad$ $p=mv$

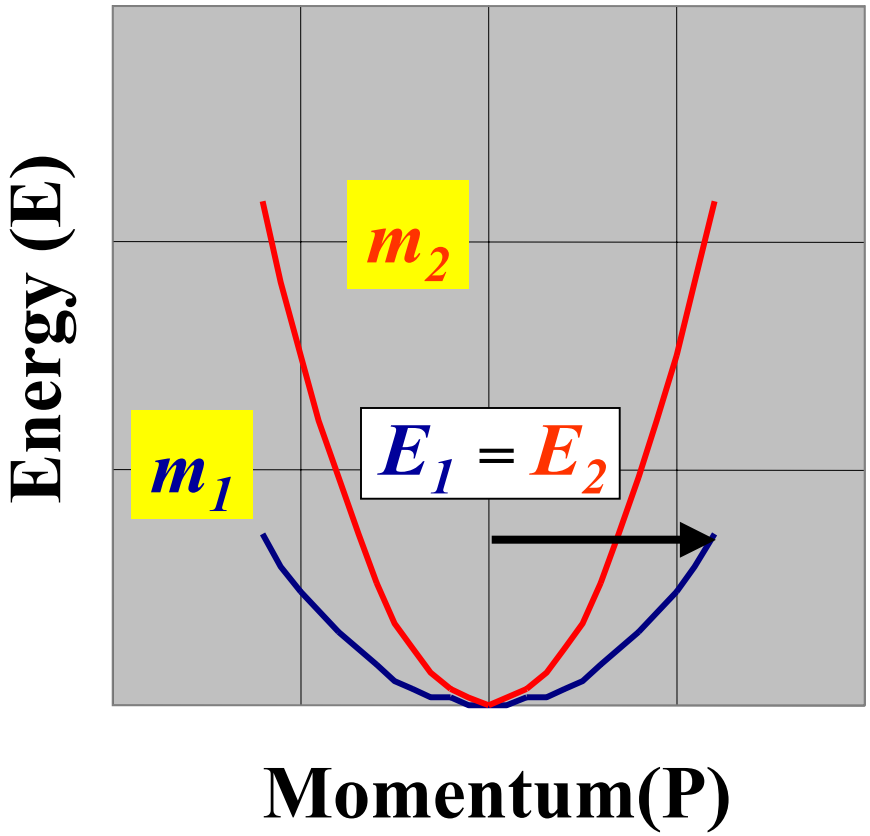
$E=p^2/2m$

$E_1=p^2/2m_1$ $\quad$ $E_2=p^2/2m_2$

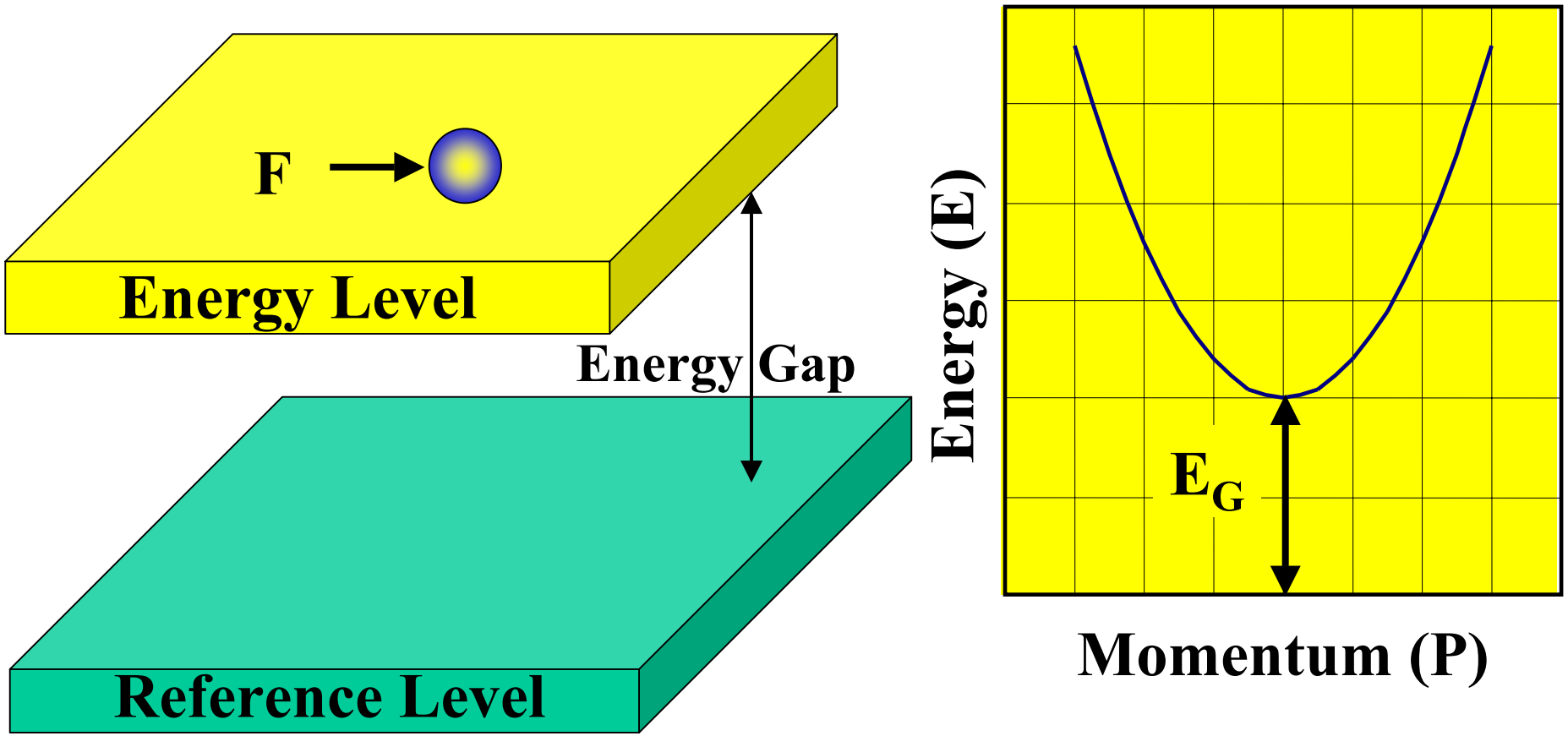
$E_1 = E_2$

$p_1 > p_2 \Rightarrow m_1 > m_2$



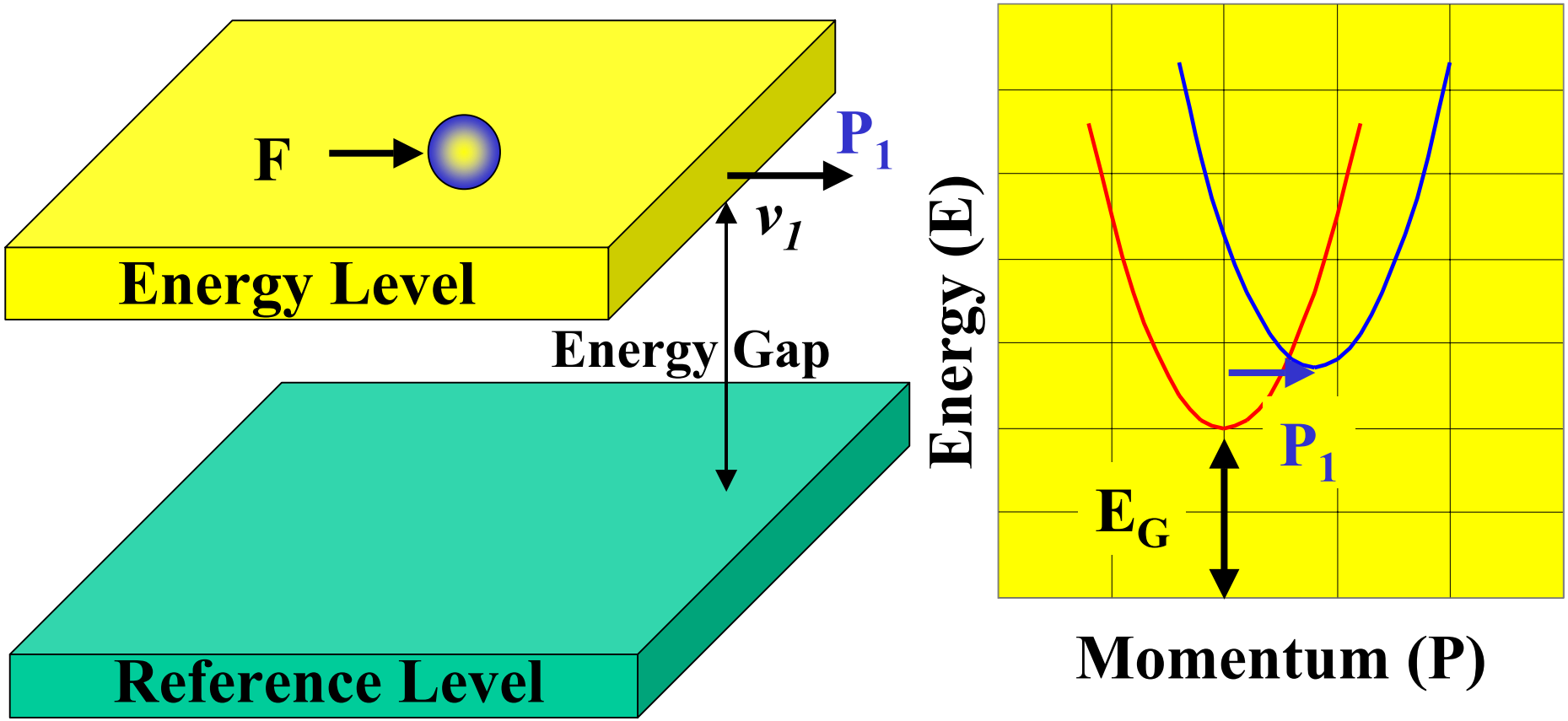


Energy Gap
(Direct Gap)



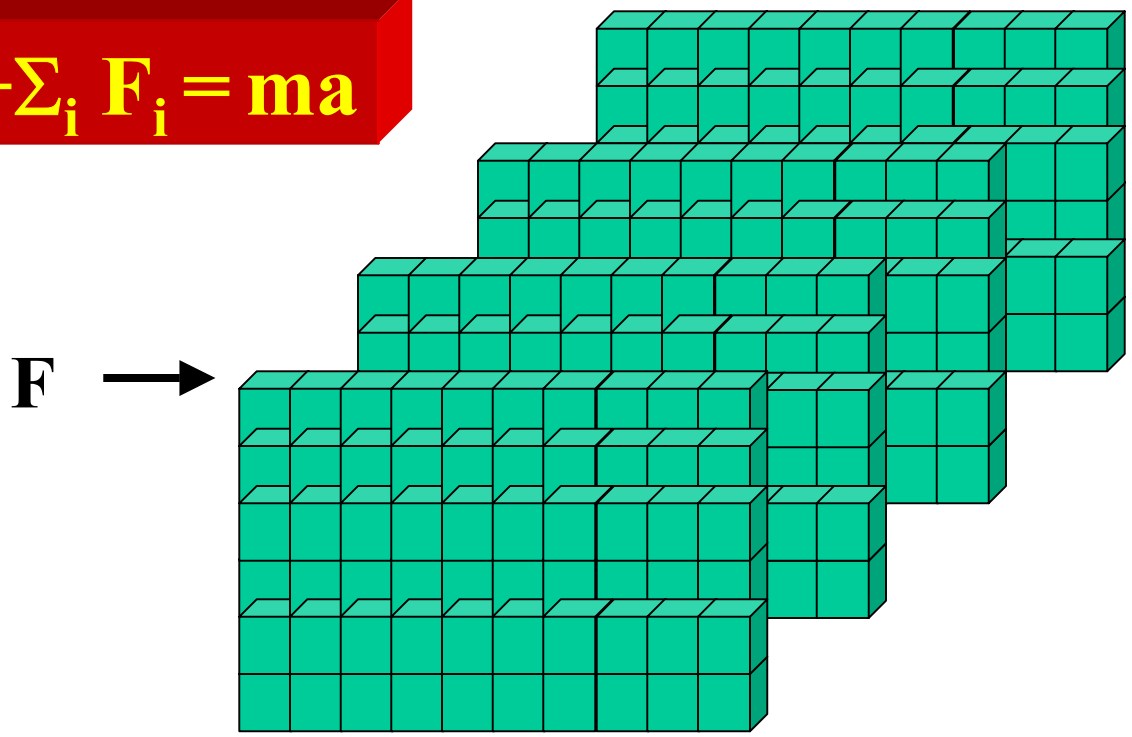
Energy Gap and Momentum Offset

(Indirect Gap)



Particle Motion in a Crystal

$F+\Sigma_i F_i = ma$



Free Space

$F=ma$

F →

Effective Mass

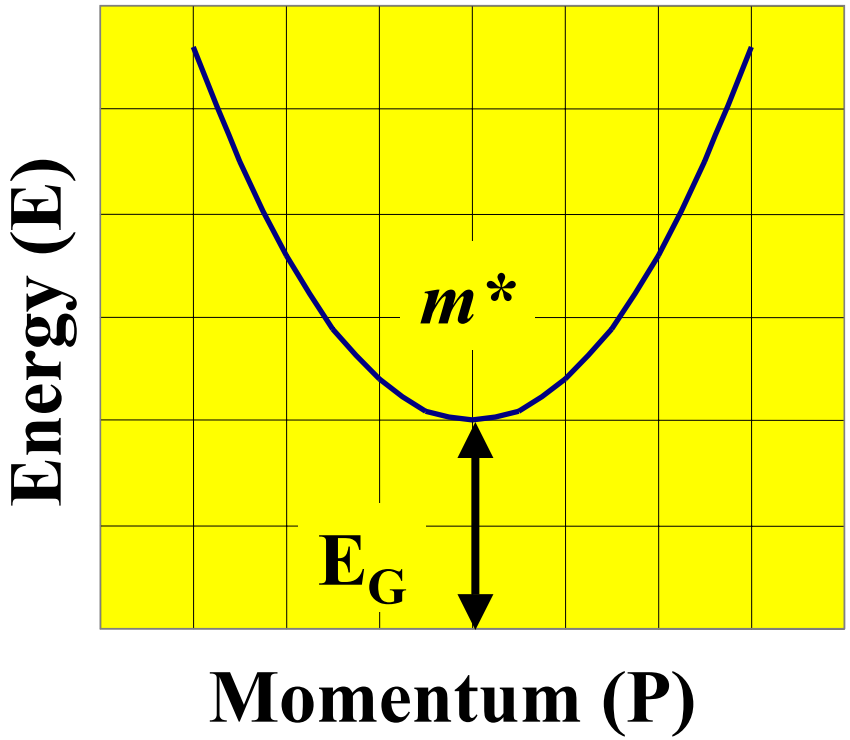
Free Space $F=ma$

Crystal $F+\Sigma_i F_i = ma$

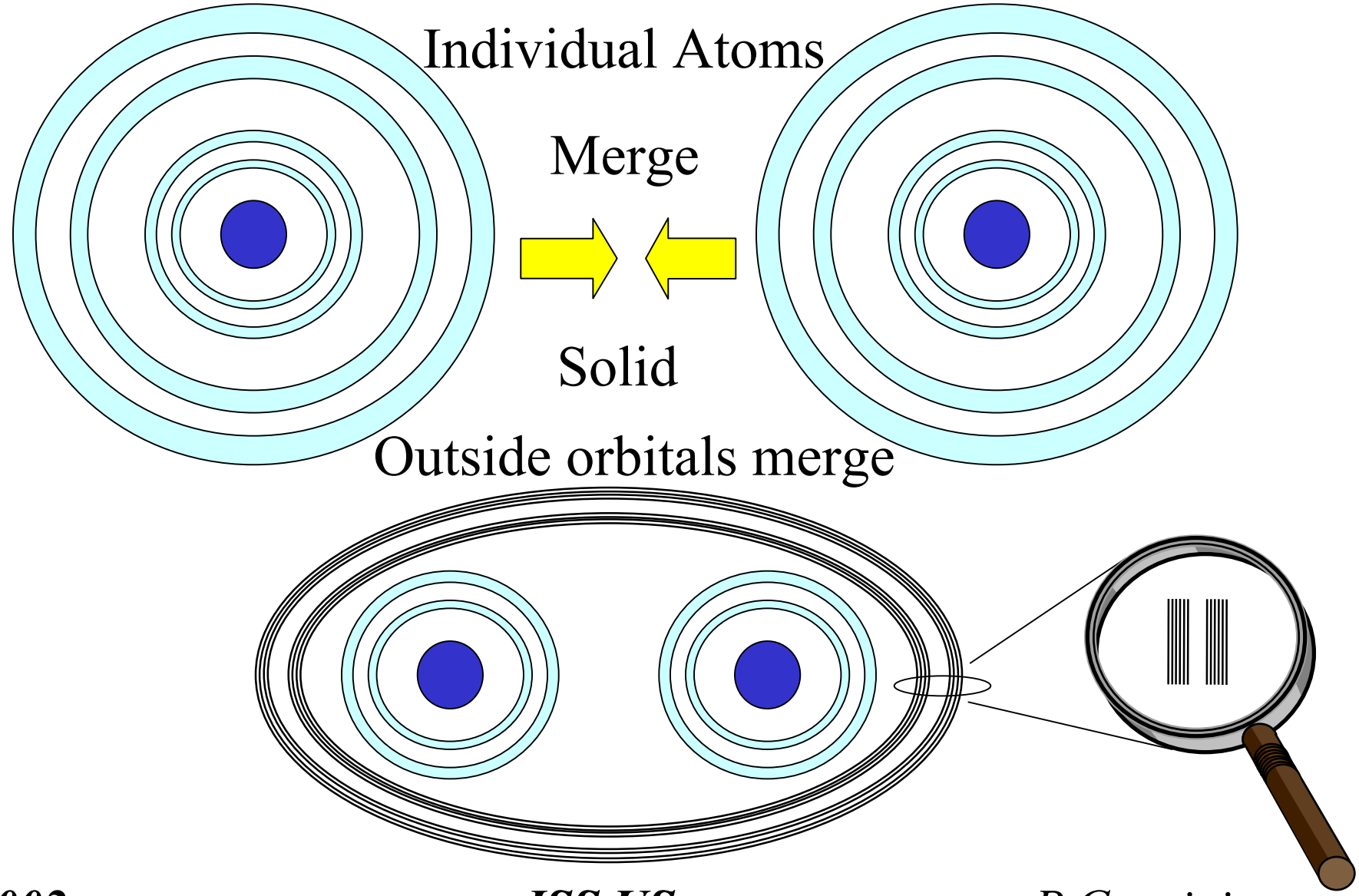
Analogy $F=m^*a$

$$m^* = \frac{\hbar}{\delta^2 E/\delta p^2}$$

In a Crystal



The making of a solid

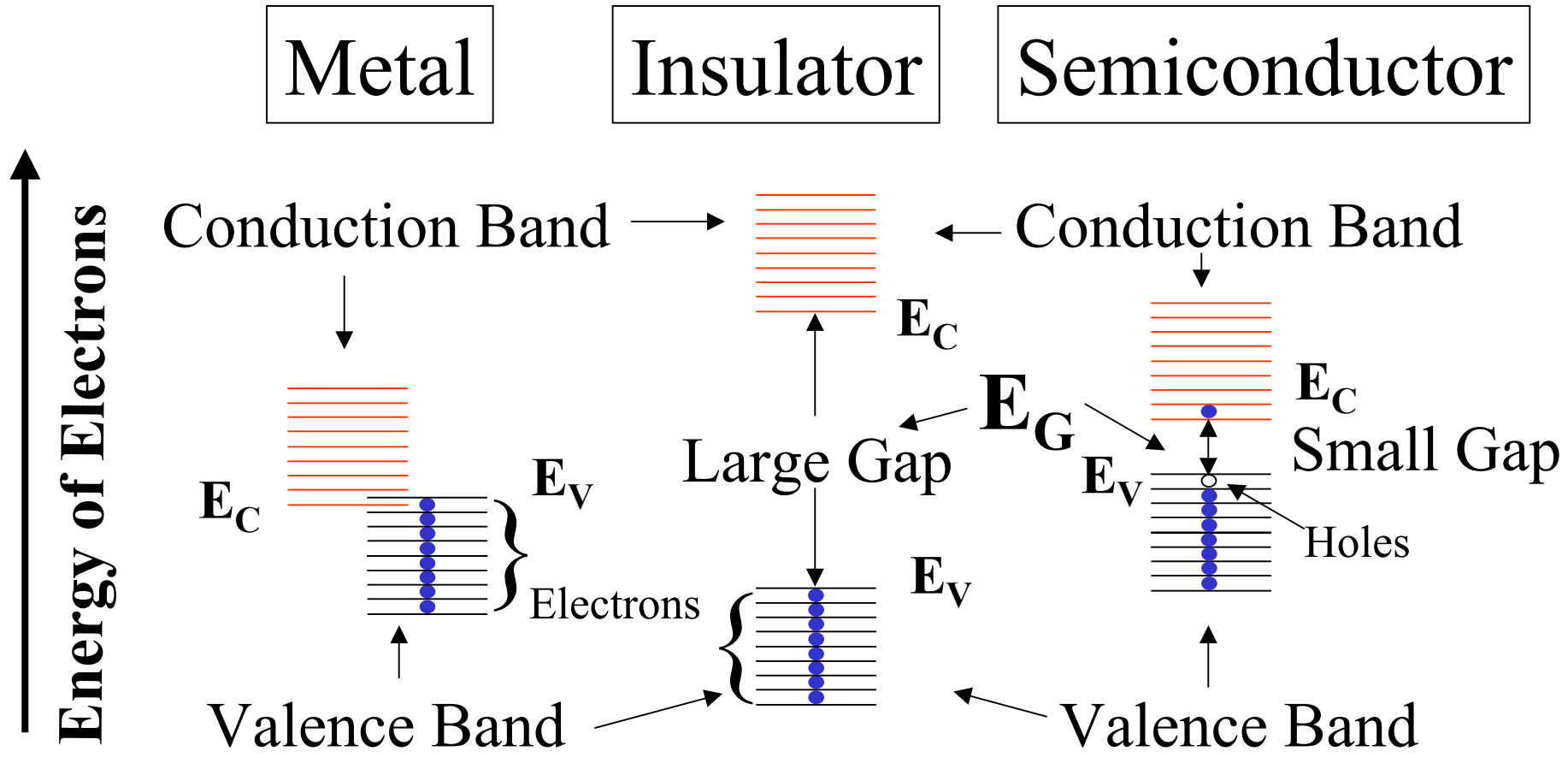


Conduction in Materials

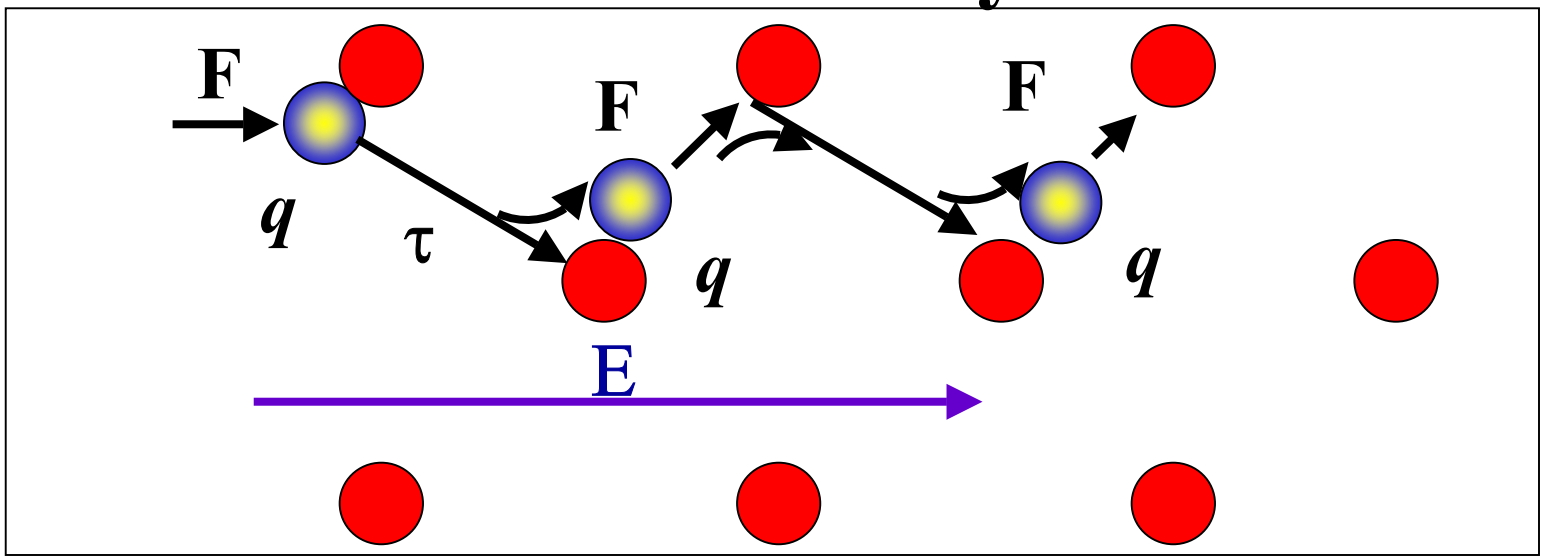
- When atoms are brought together, under appropriate conditions, they form a solid, regular structure called crystal
- When atoms are brought together and form a solid crystal, the outside electrons' orbitals merge and form energy bands
- When the outermost *bands overlap* (superimpose) and contain many electrons->*metal* (high conductivity)
- When the two outmost outside *bands* are *far apart* =>*insulator* (low conductivity)
- When the two outmost outside *bands* are *close* but still separated=> *semiconductor* (intermediate conductivity)

Conductivity= the ability to conduct current

Band Structure and Conduction in Solids



Motion in a Crystal



In Free Space

$F = qE$ $\quad qE = ma$

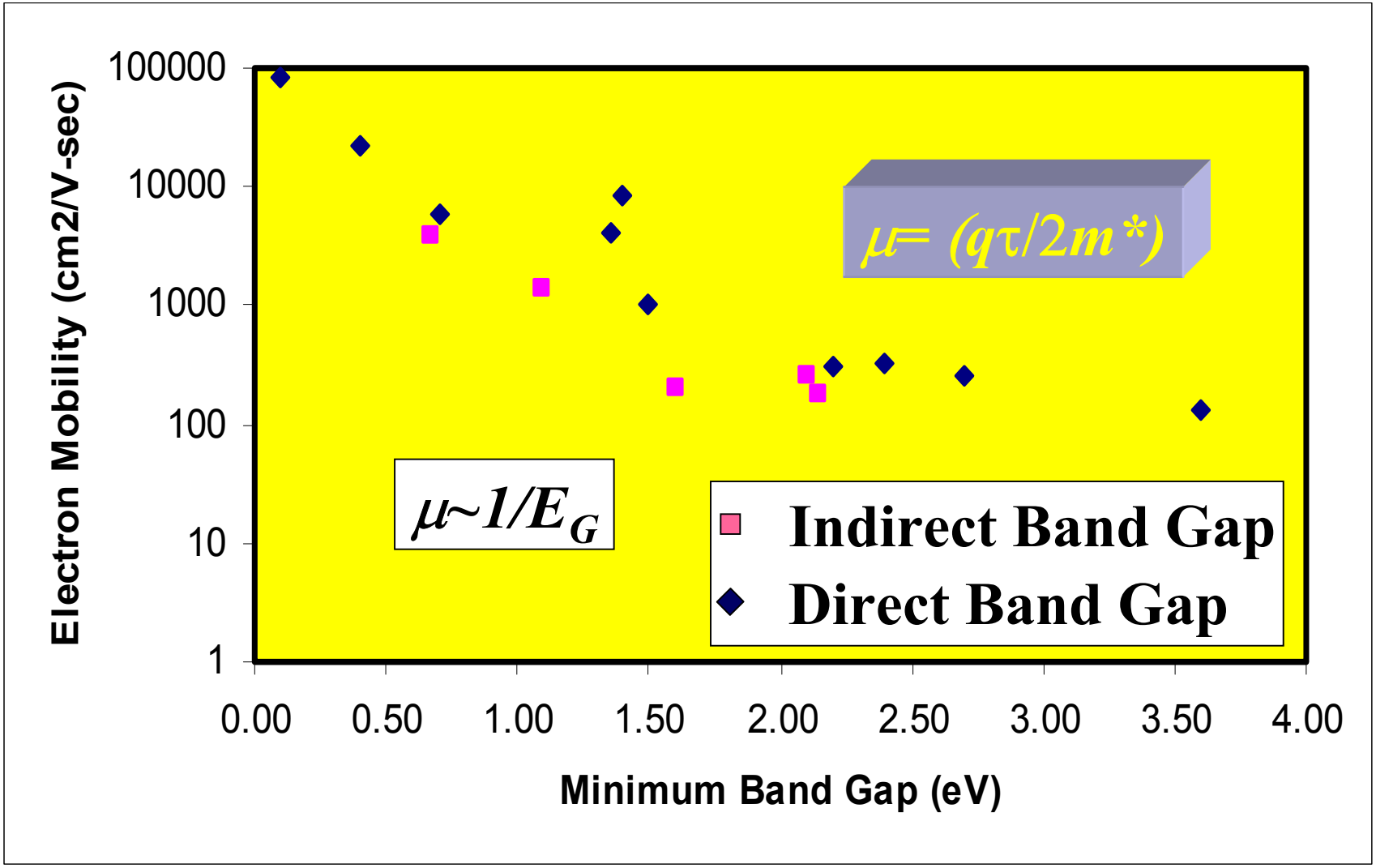
In Semiconductor

$qE = m^*a$ $\quad a = qE/m^*$

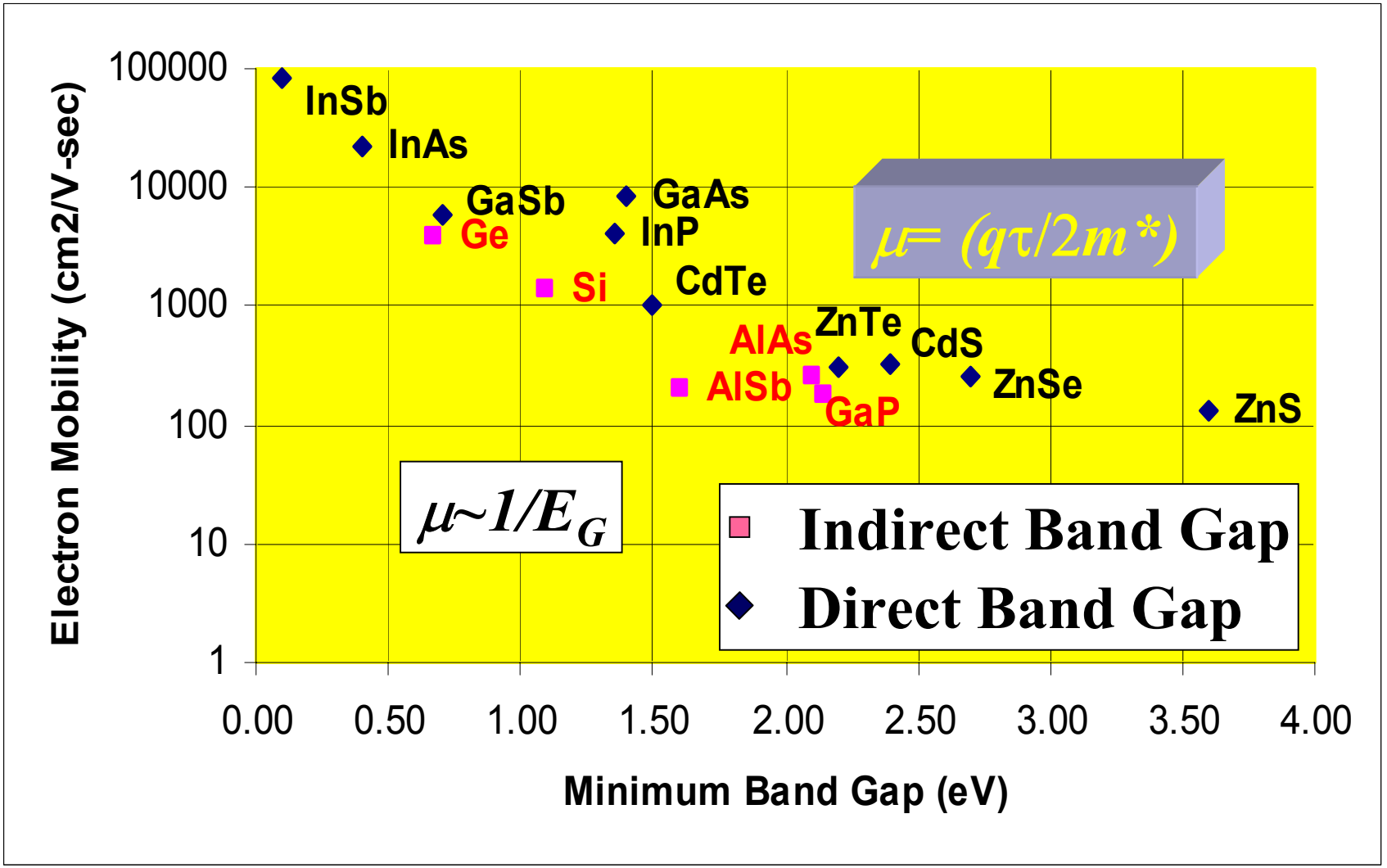
$V_{max} = a\tau = (qE/m^*)\tau \rightarrow \langle v \rangle = [0 + V_{max}]/2 \rightarrow$

$\rightarrow \langle v \rangle = (q\tau/2m^*)E \rightarrow \langle v \rangle = \mu E$ $\quad \mu = (q\tau/2m^*)$

Mobility Increase with E_G Reduction



Mobility Increase with E_G Reduction



Summary of Solid State Physics Refresher

- Energy and Momentum of a particle moving in free space are related by the formula: $E=p^2/2m$
- Energy and Momentum of a particle moving in a crystal are related by the formula: $E=p^2/2m^*$
- The motion of a particle in a crystal is characterized by:

$\langle v \rangle = \mu E$

$\mu = (q\tau/2m^*)$

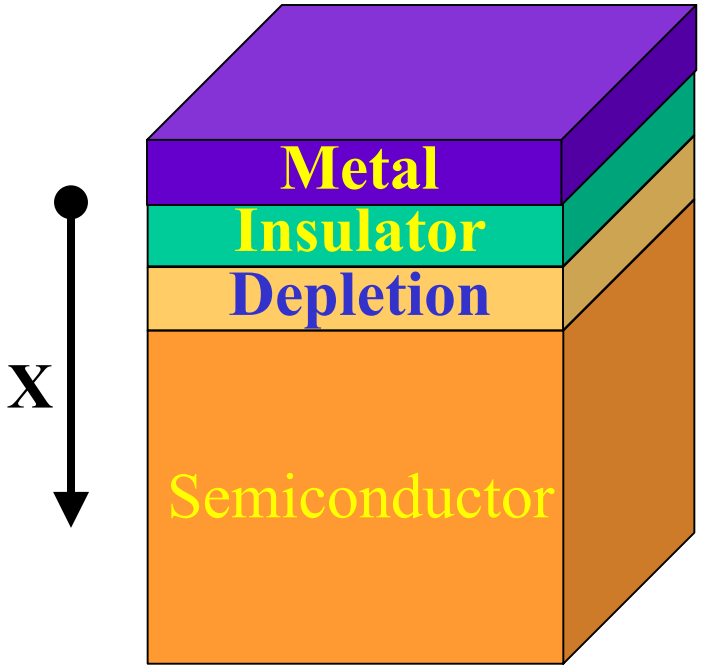
- Conduction is controlled by the energy band structure:
  - No Energy Gap=Metal
  - Large Energy Gap=Insulator
  - Small Energy Gap=Semiconductor

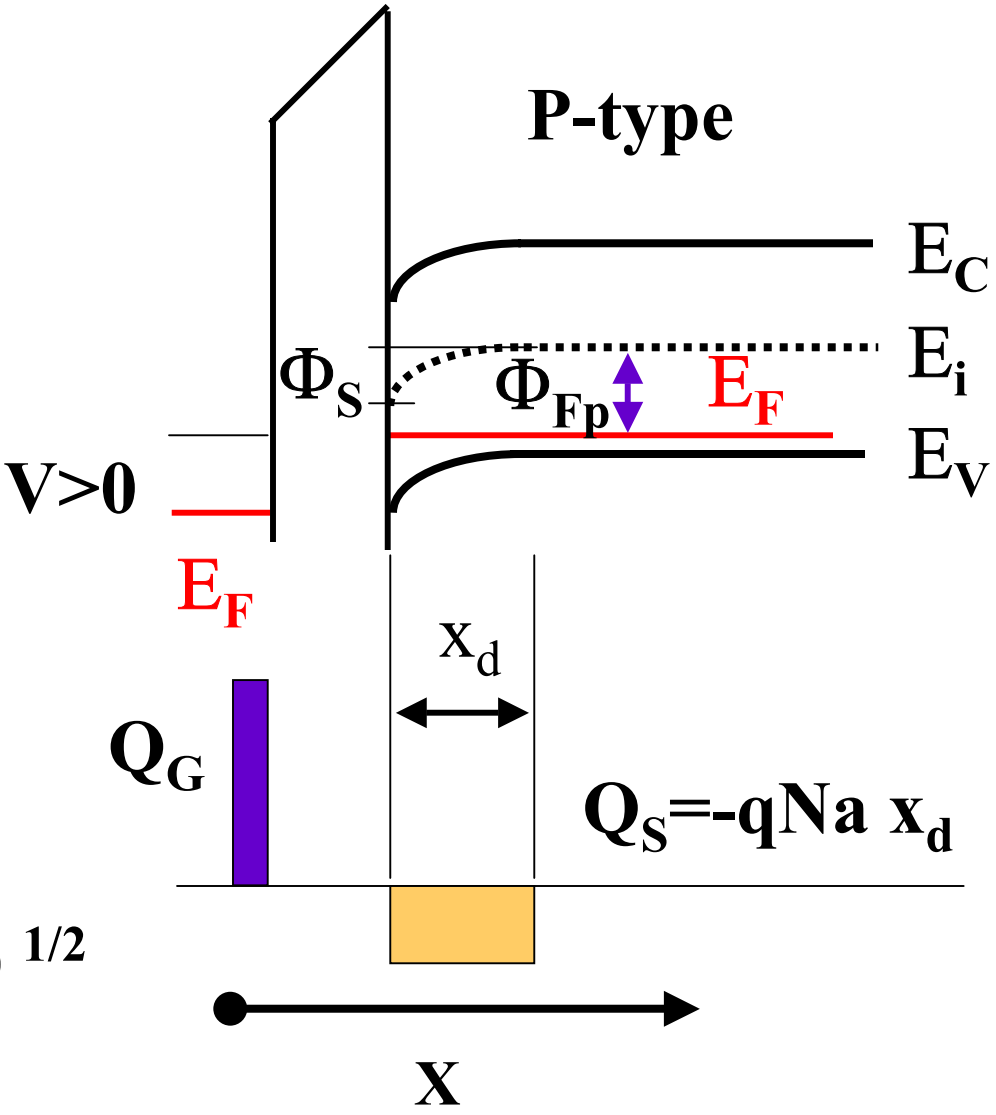
E_G

Agenda

- Solid State Physics Refresher
- ***MOS Device Physics Refresher***
- Classical CMOS Limitations
- Non-classical CMOS
- New Emerging Technologies
- Conclusions

Semiconductor Surface in Depletion

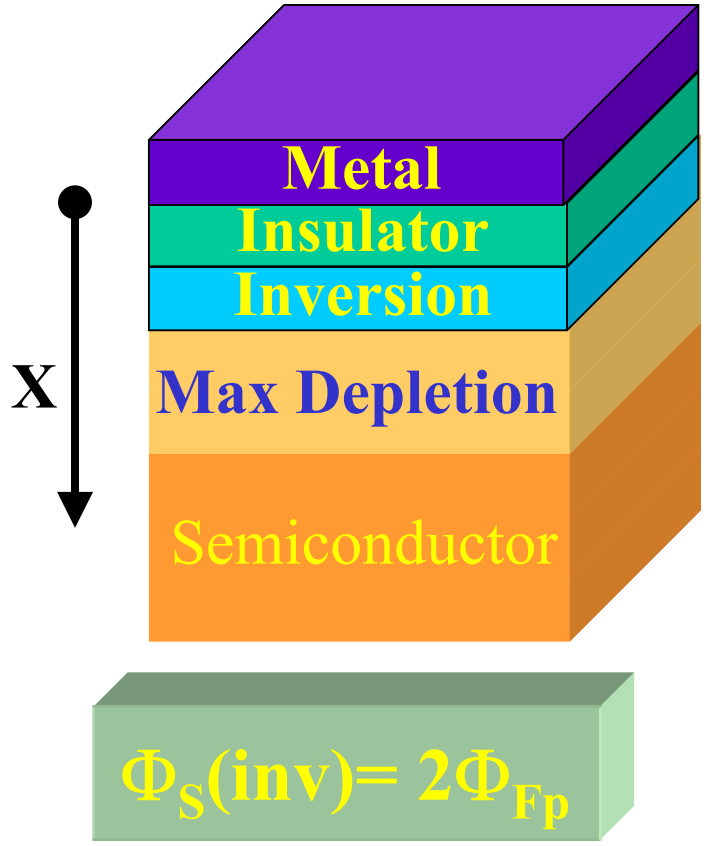




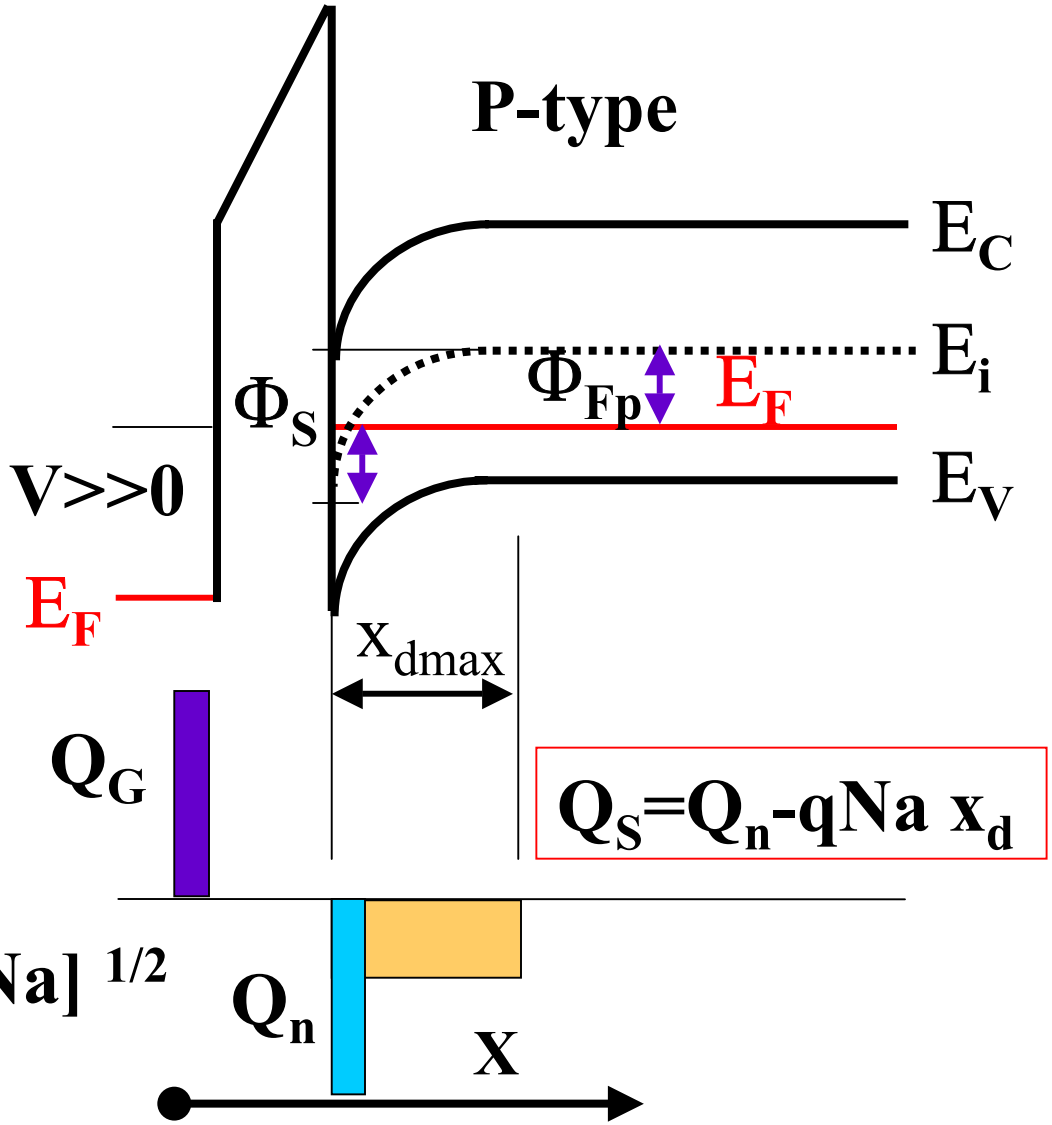
$$\Phi_S = qNa\, x_d^{\,2} / 2\varepsilon_o\, \varepsilon_s$$

$$x_d = (2\varepsilon_o\, \varepsilon_s\, \Phi_S / qNa)^{1/2}$$

Semiconductor Surface in Inversion

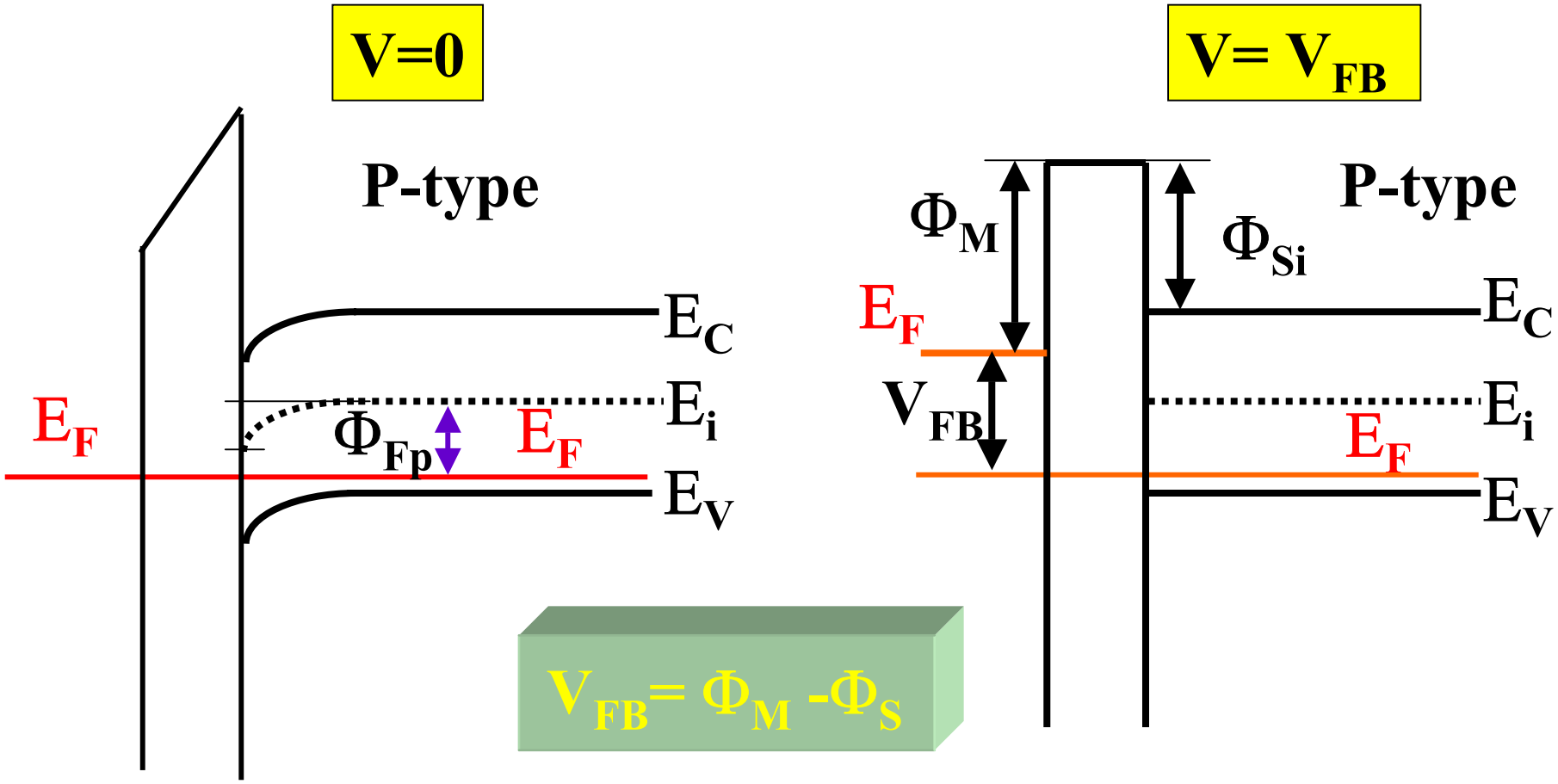


$\Phi_S(inv) = 2\Phi_{Fp}$



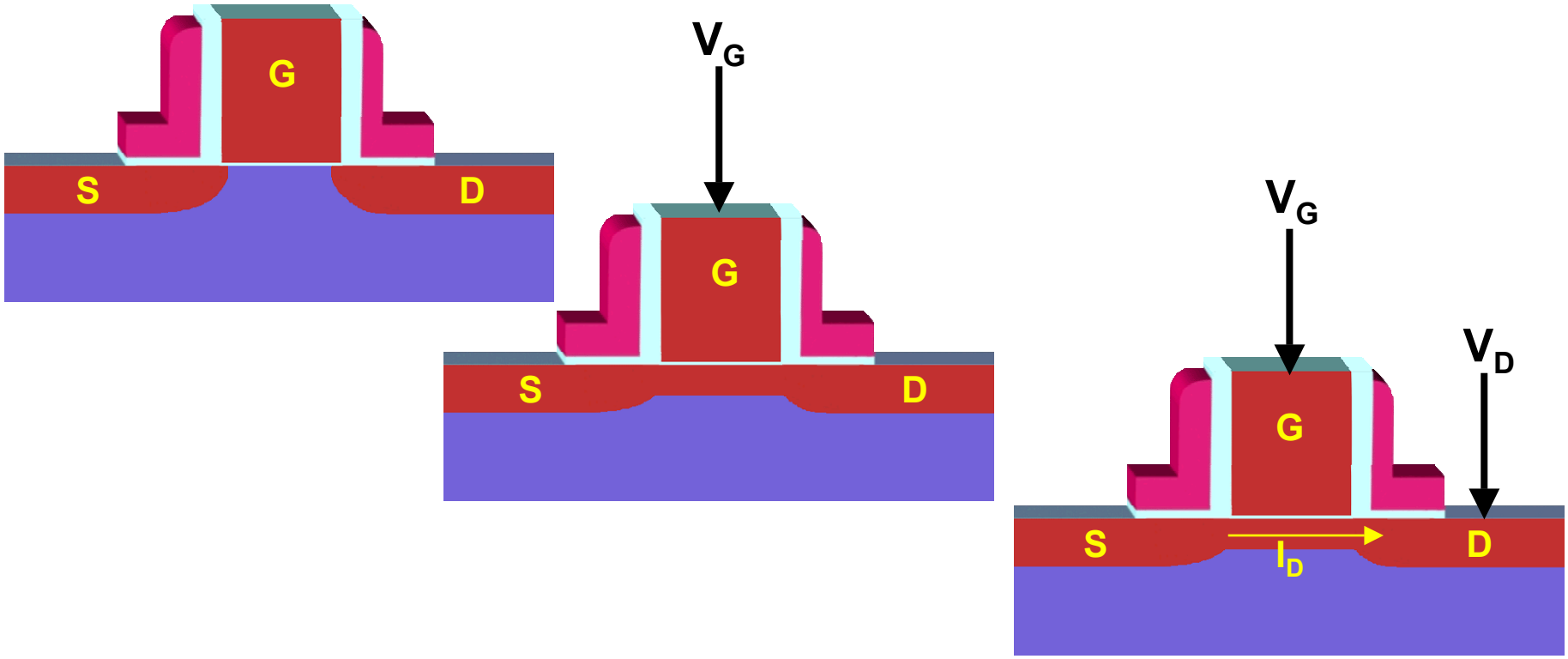
$$x_{d\,Max} = [2\varepsilon_o\,\varepsilon_s\,(2\Phi_{Fp}) / qNa]^{1/2}$$

Work Function Difference



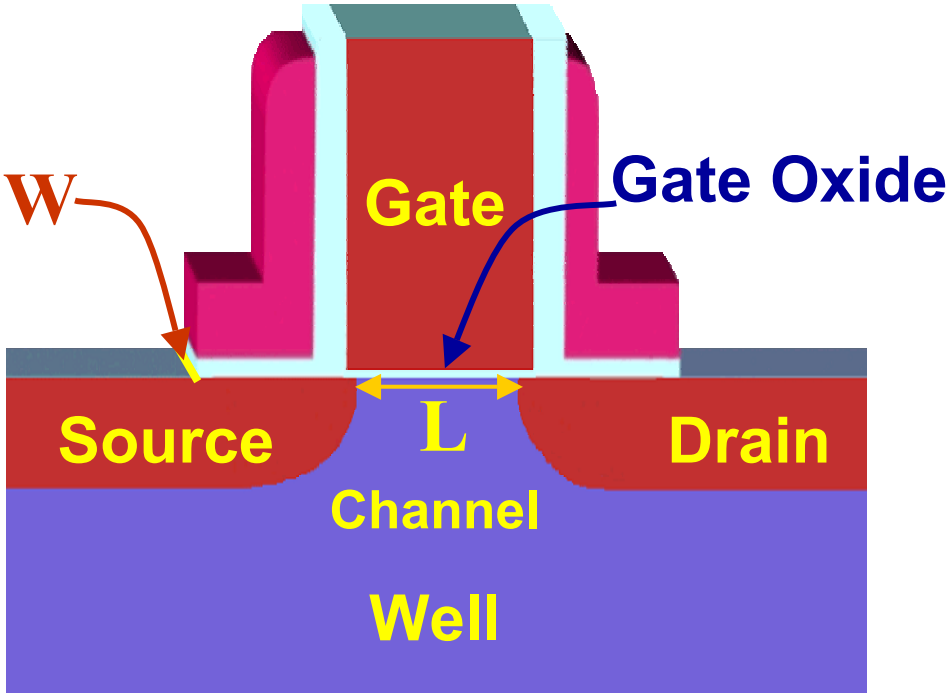
Flat-band Voltage

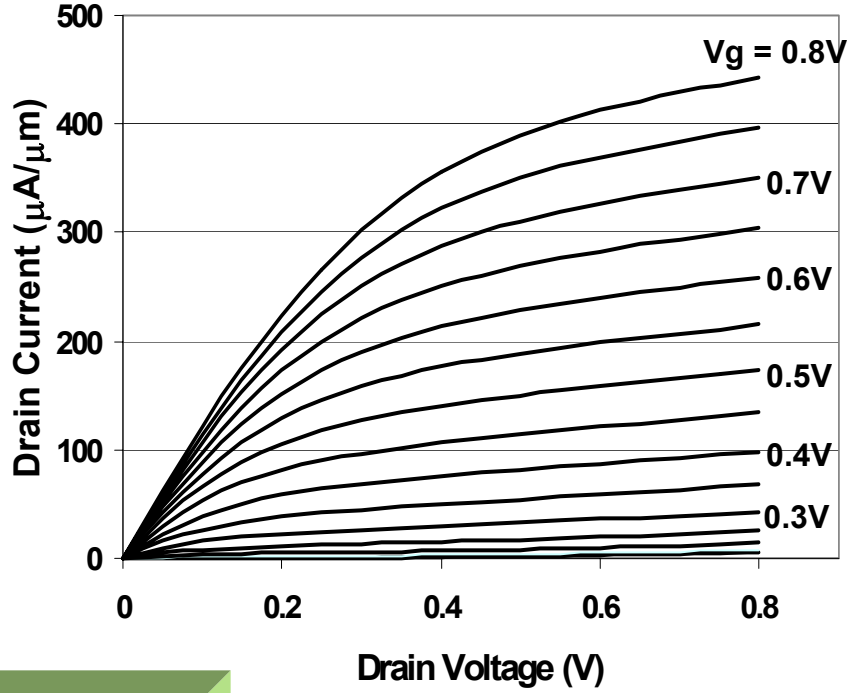
MOS transistor: Threshold Voltage



$$V_T = V_{FB} + 2\Phi_{Fp} + [2\,\varepsilon_O\,\varepsilon_s\,qNa(2\Phi_{Fp})]^{1/2}/C_{ox} \sim V_{FB} + 2\Phi_{Fp}$$

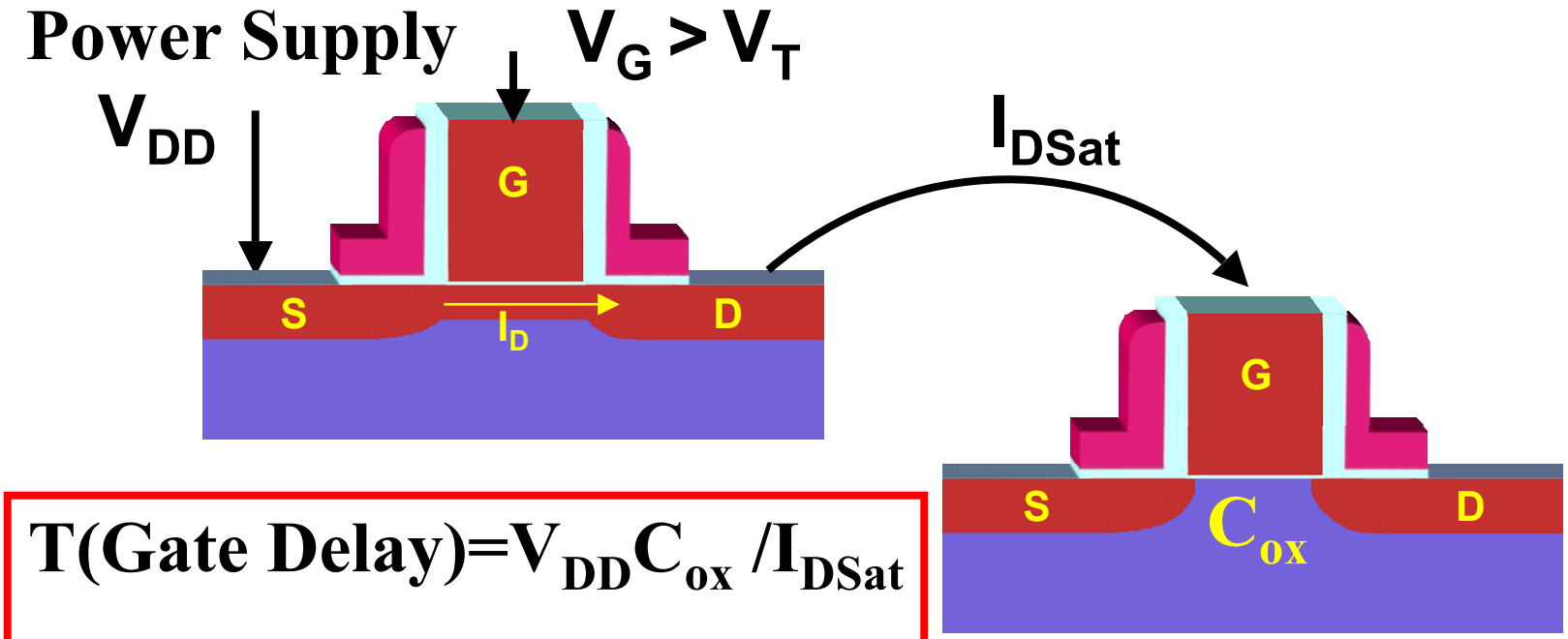
MOS transistor: Saturation Current





$$I_{DSat} \sim \frac{1}{2} \mu C_{ox} \frac{(W)}{Lg} (V_G - V_T)^2$$

Loaded Transistor: F_{Max} and Power



$T(\text{Gate Delay}) = V_{DD} C_{ox} / I_{DSat}$

$F_{Max} = 1/T = I_{DSat} / V_{DD} C_{ox}$

$\text{Power} = V_{DD}\, I_{DSat} = V_{DD}\,(V_{DD} C_{ox})/T = V_{DD}^2\, C_{ox}\, F_{Max}$

Transistor Trade-offs

Lg	μ	C_{ox}	V_{DD}	V_T

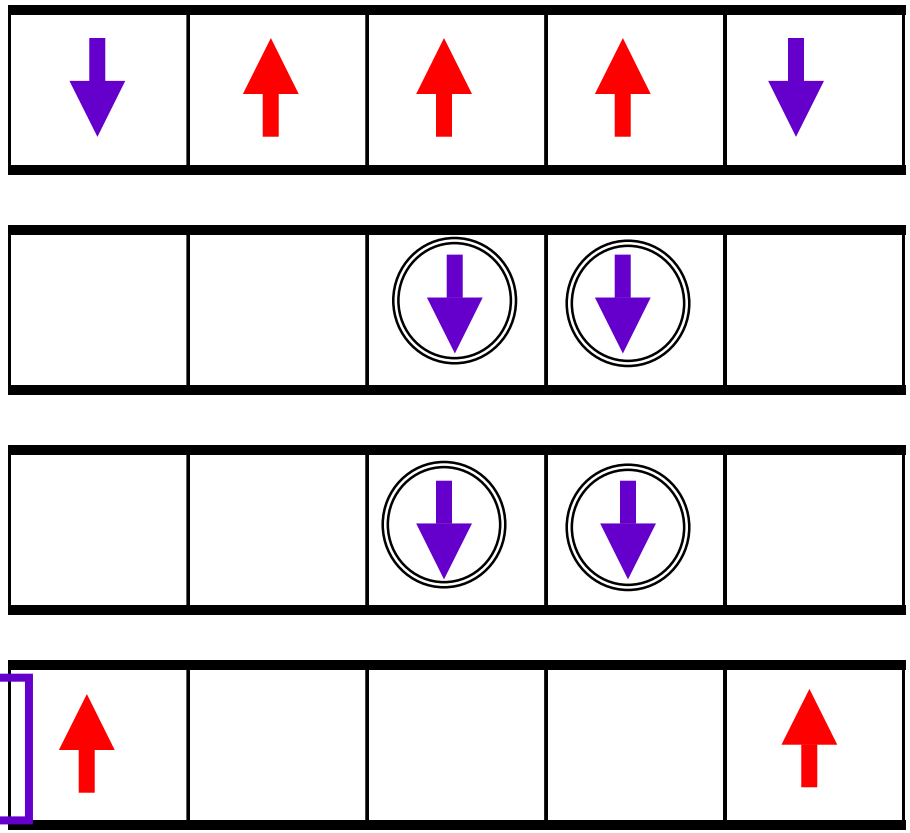
$$I_{DSat} \sim \frac{1}{2} \mu C_{ox} \frac{W}{Lg} (V_{DD} - V_T)^2$$

$$F_{Max} = I_{DSat} / V_{DD} C_{ox}$$

$$Power = V_{DD}^2 C_{ox} F_{Max}$$

$$I_{OFF} \rightarrow V_{PT} = Lg^2 qNa / 2 \varepsilon_o \varepsilon_s$$

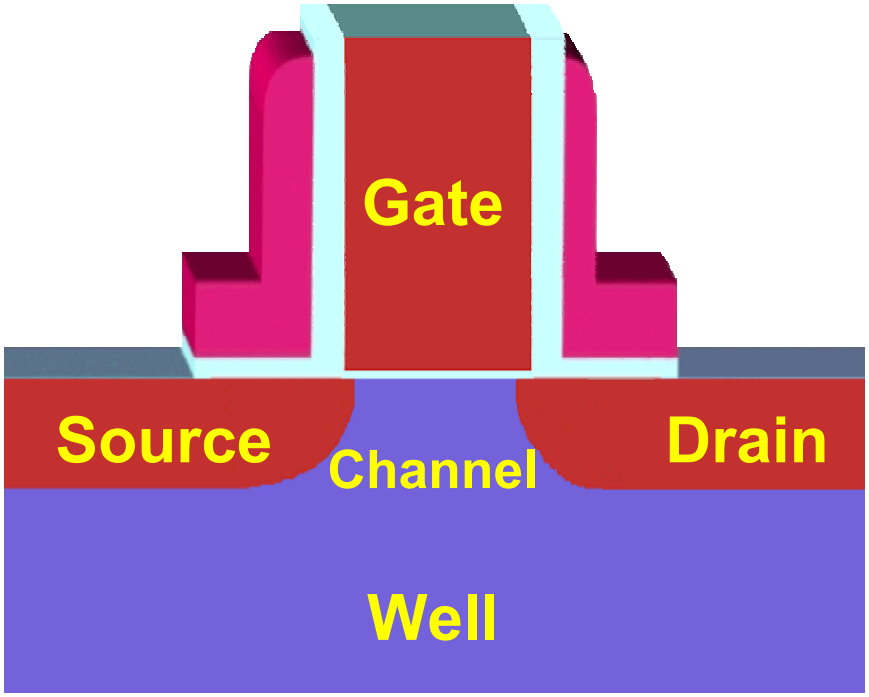
$$V_T \sim V_{FB} + 2\Phi_{Fp}$$



Maximize

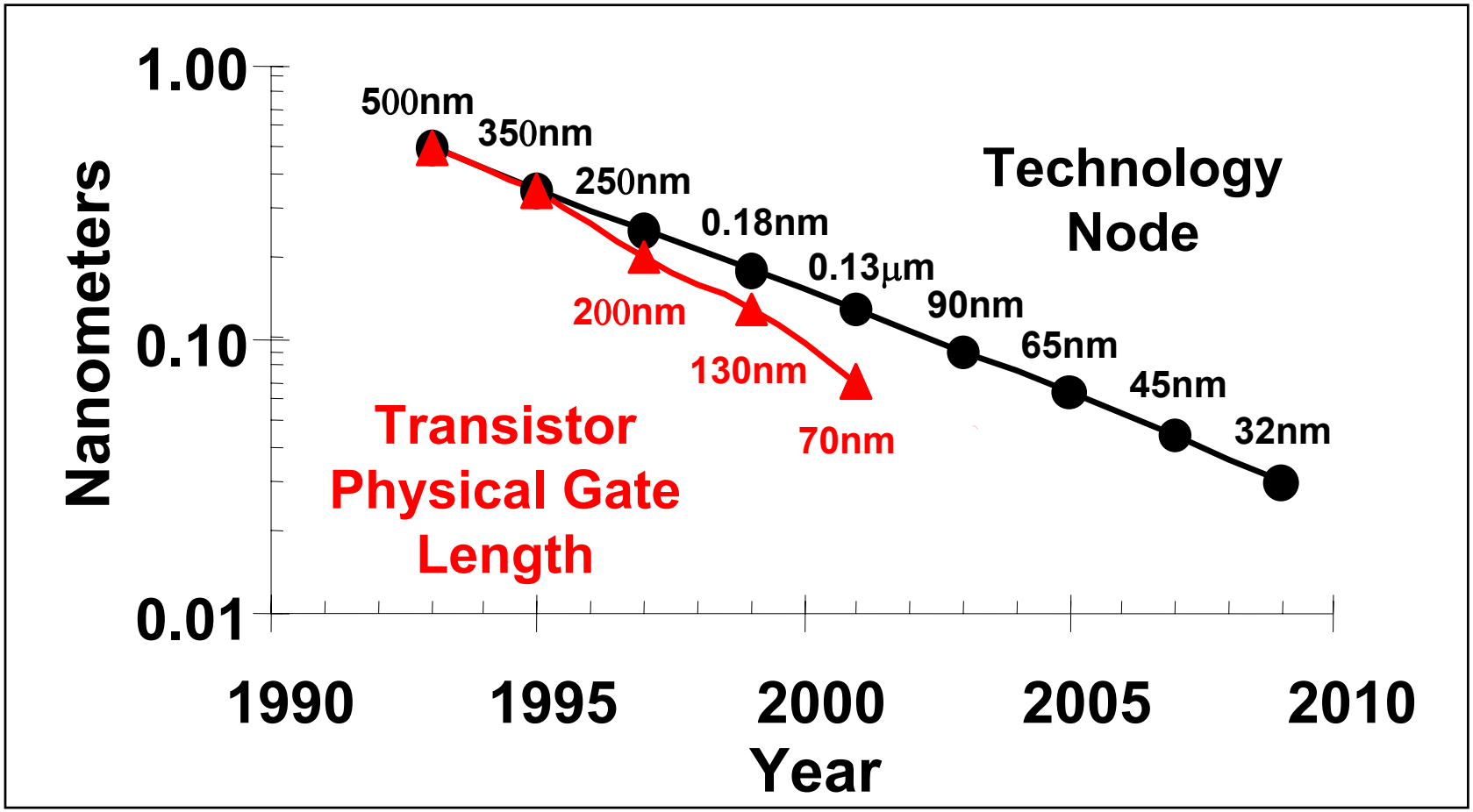
Minimize

MOS Transistor Optimization

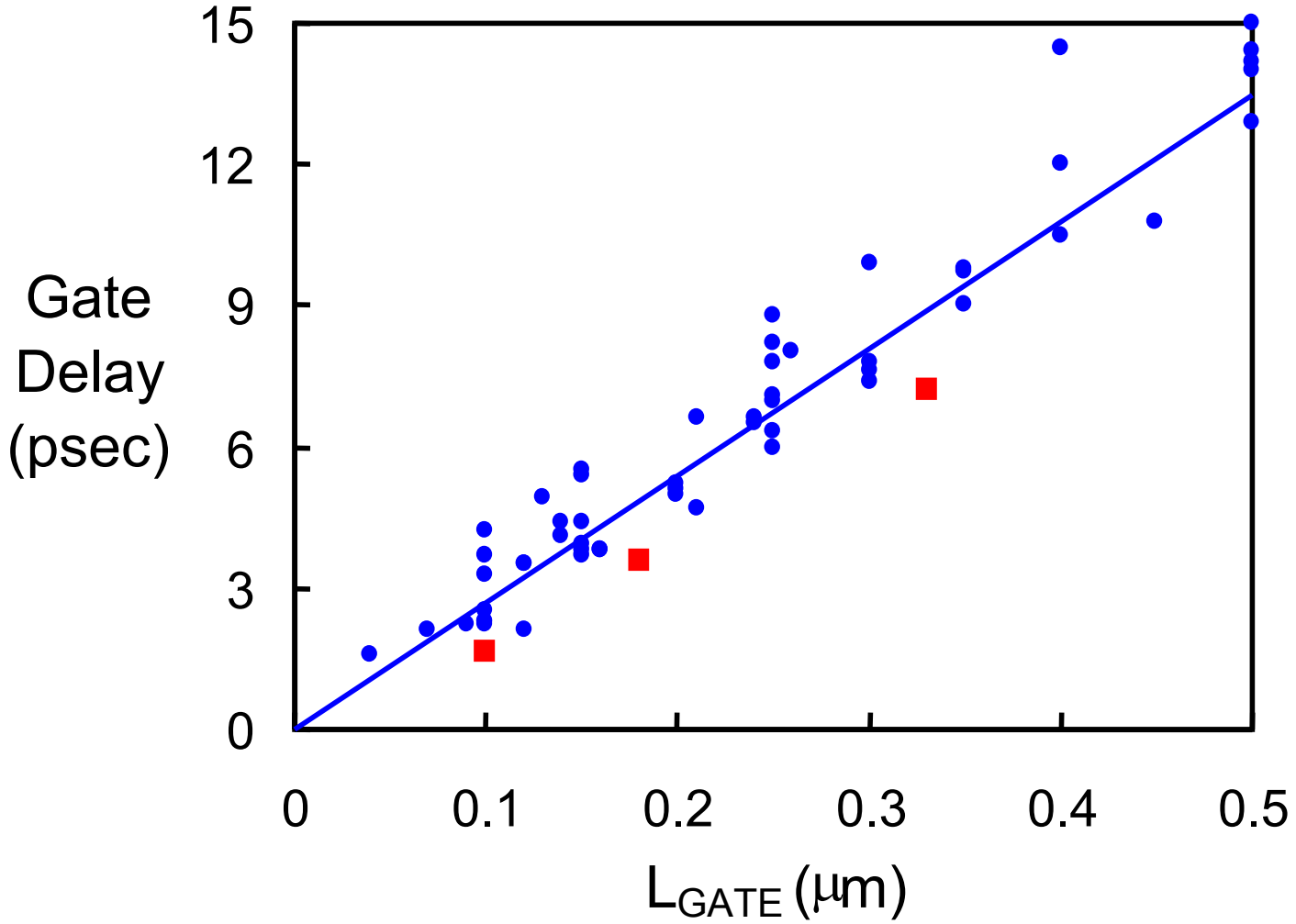


- Idsat
  - Reduce Lg
  - Reduce Tox
- F_{max}
  - Reduce Xj
- Power
  - Reduce V_{DD}
- Ioff, Vt
  - Increase Doping
- Latch Up, Soft Error
  - Well

Transistor Physical Gate Length Trend



Transistor CV/I Delay Trend



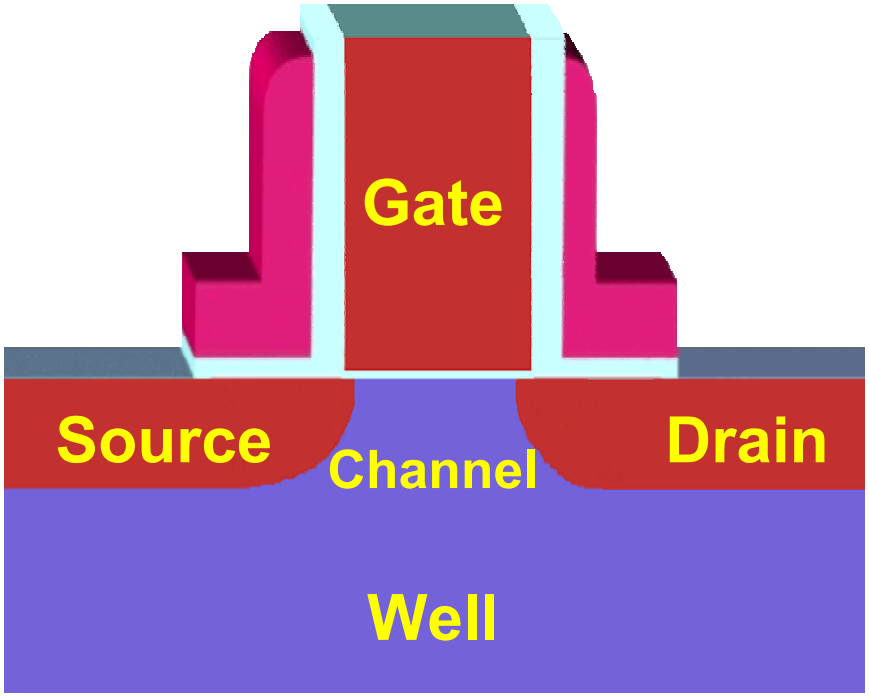
Summary of MOS Device Physics Refresher

- **I_{DSat}, F_{Max}, Power, I_{OFF}** and **V_T** are the fundamental parameters describing MOS performance
- **Lg** (reduction) determines the speed **(F_{Max})** of an MOS device
- Reduction of **V_{DD}** minimizes power consumption
- Both higher doping and increased **Lg** reduce **I_{OFF}**
- Threshold voltage **V_T** is controlled by surface doping and by work function difference (gate conductor to silicon)

Agenda

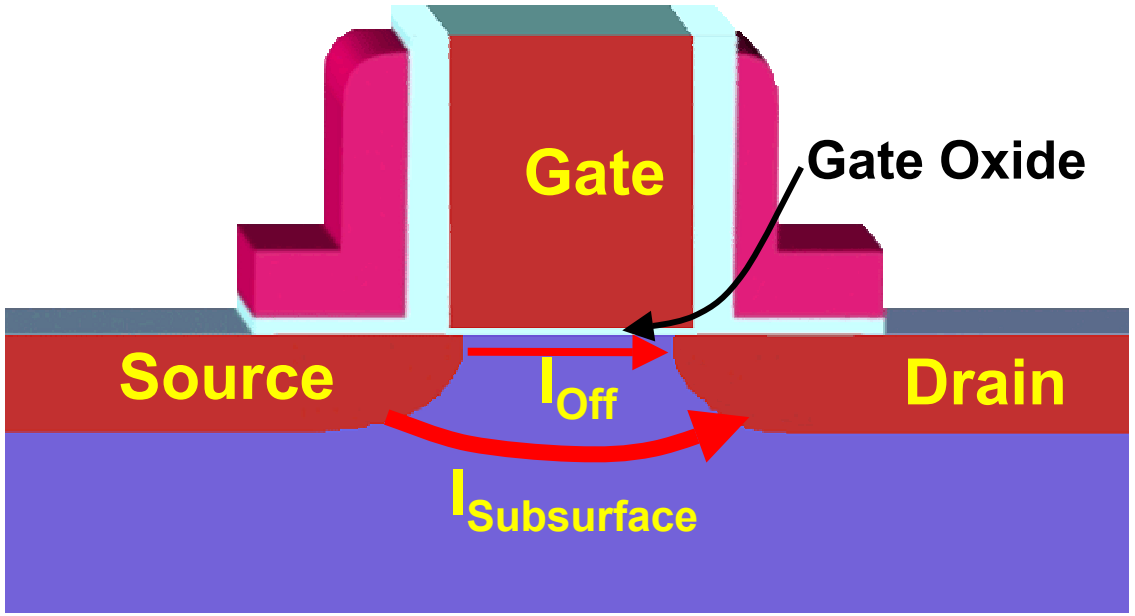
- Solid State Physics Refresher
- MOS Device Physics Refresher
- ***Classical CMOS Limitations***
- Non-classical CMOS
- New Emerging Technologies
- Conclusions

MOS Transistor Limitations



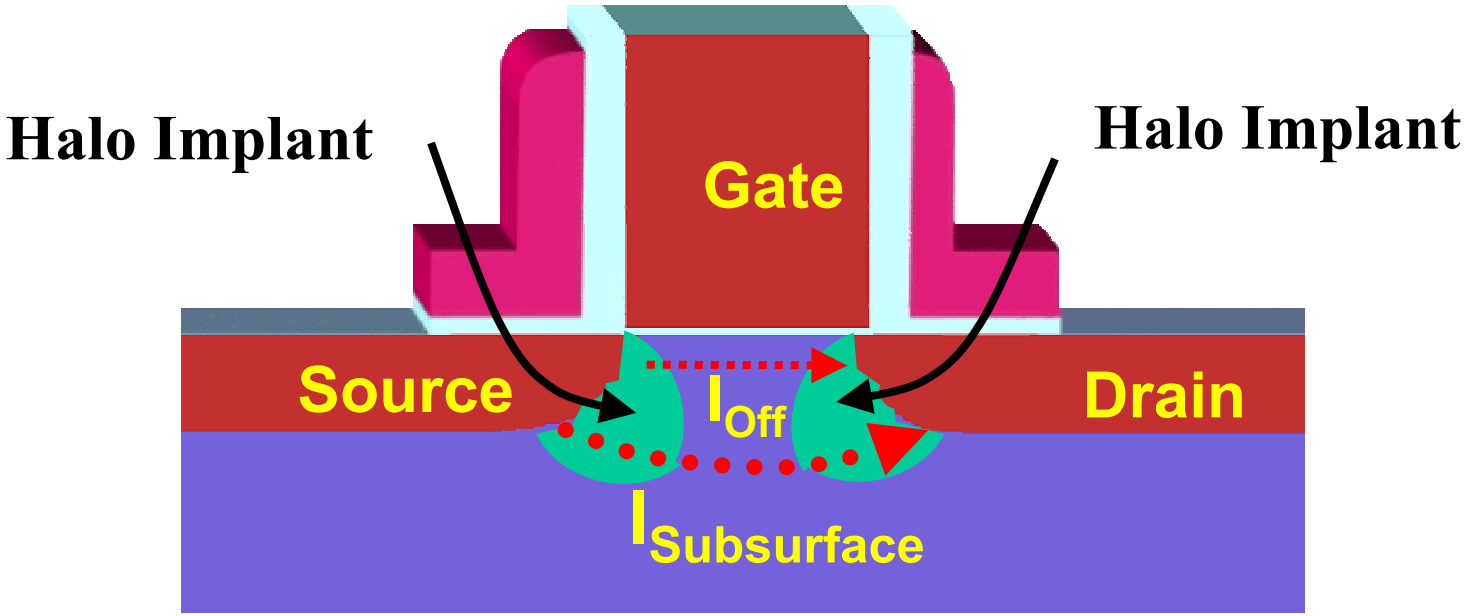
- Excessive
  - Off State I Leakage
  - Gate Oxide Leakage
- Increasing
  - Parasitic Resistance
  - Junction Capacitance
- Increasing Doping
  - Mobility Degradation
- Conductive Substrate
  - Punch-Through

Challenges: Off-state Leakage



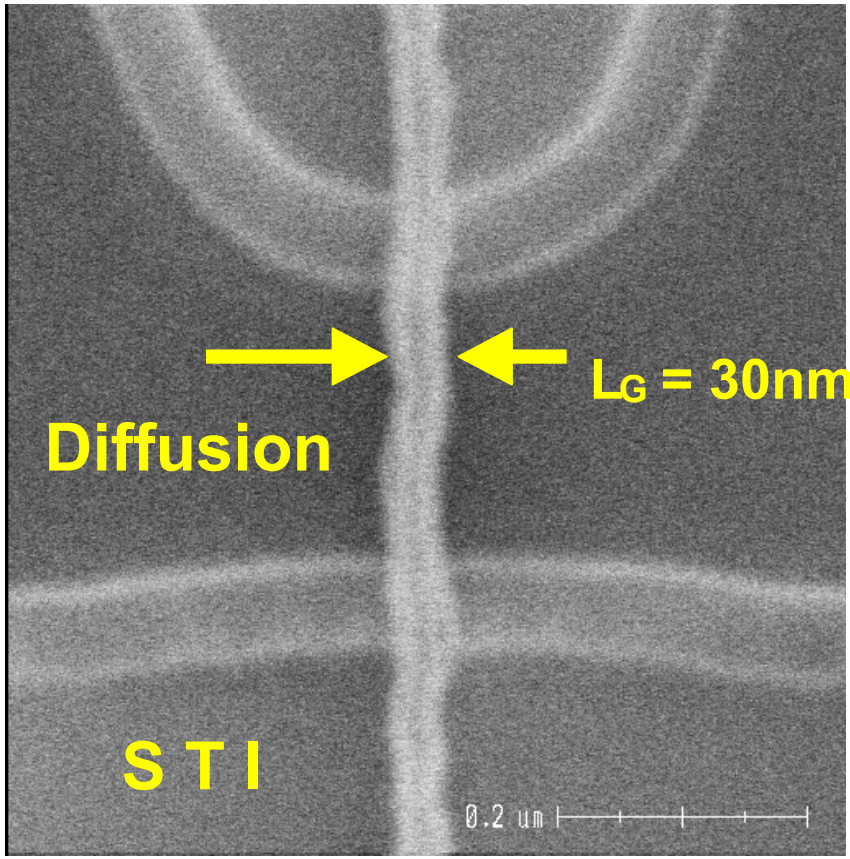
- **Off-state (Sub-threshold) leakage:**
  - Ideally, current only flows across the channel (directly beneath the gate) from source to drain when the transistor is turned on
  - If current flows under the channel when the transistor is turned off, it is called Off-state (or Sub-threshold) leakage.
  - Sub-threshold leakage consumes power in the standby or off state.
  - A leaky device requires a higher operating voltage

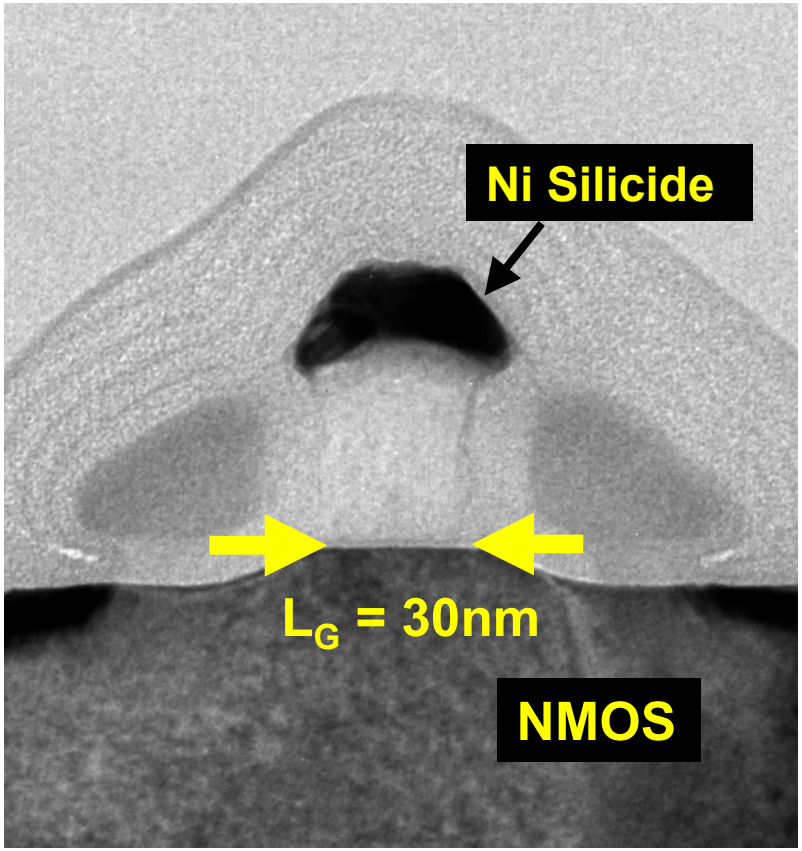
Off-state Leakage Reduction



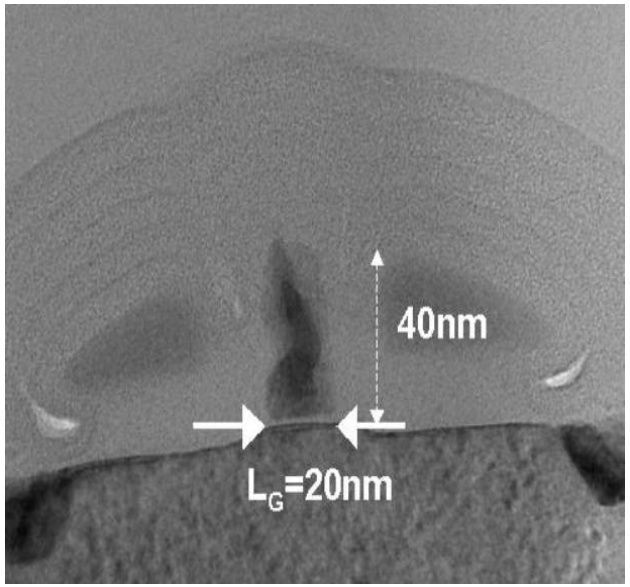
- **Off-state (Sub-threshold) leakage:**
  - Ideally, current only flows across the channel (directly beneath the gate) from source to drain when the transistor is turned on
  - If current flows under the channel when the transistor is turned off, it is called Off-state (or Sub-threshold) leakage.
  - Sub-threshold leakage is reduced by the Halo implant.

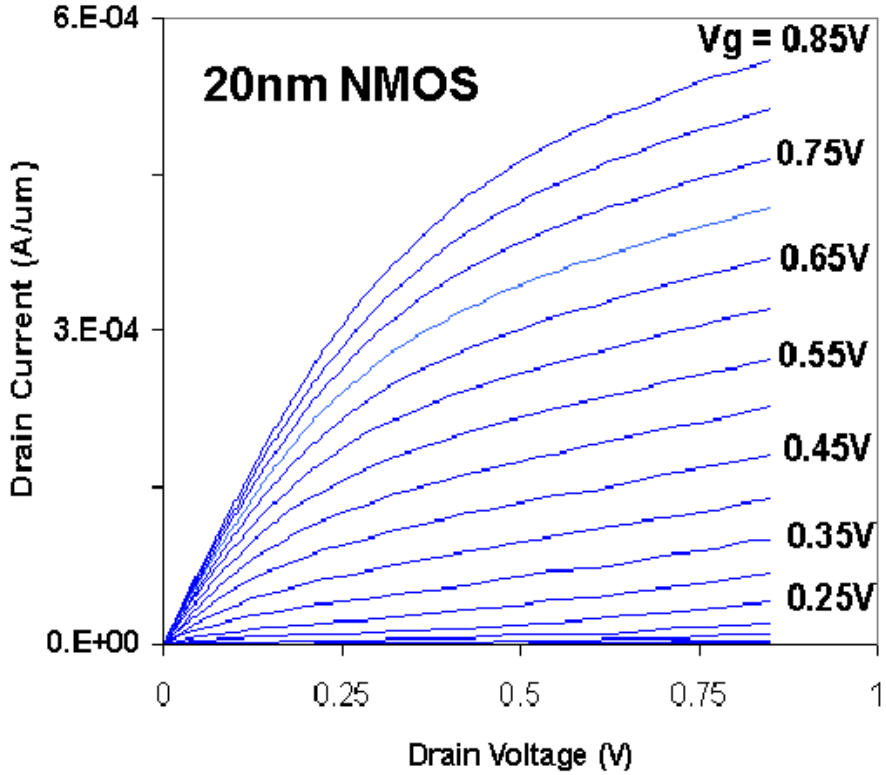
Intel's 30nm Transistor
(Dec 2000)



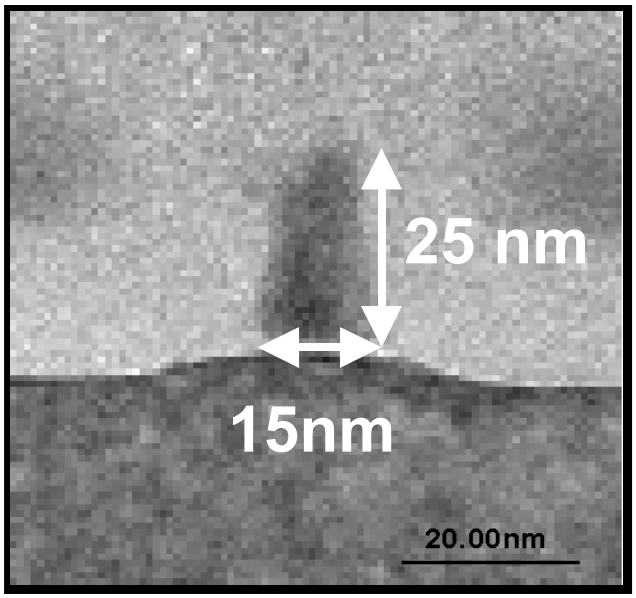


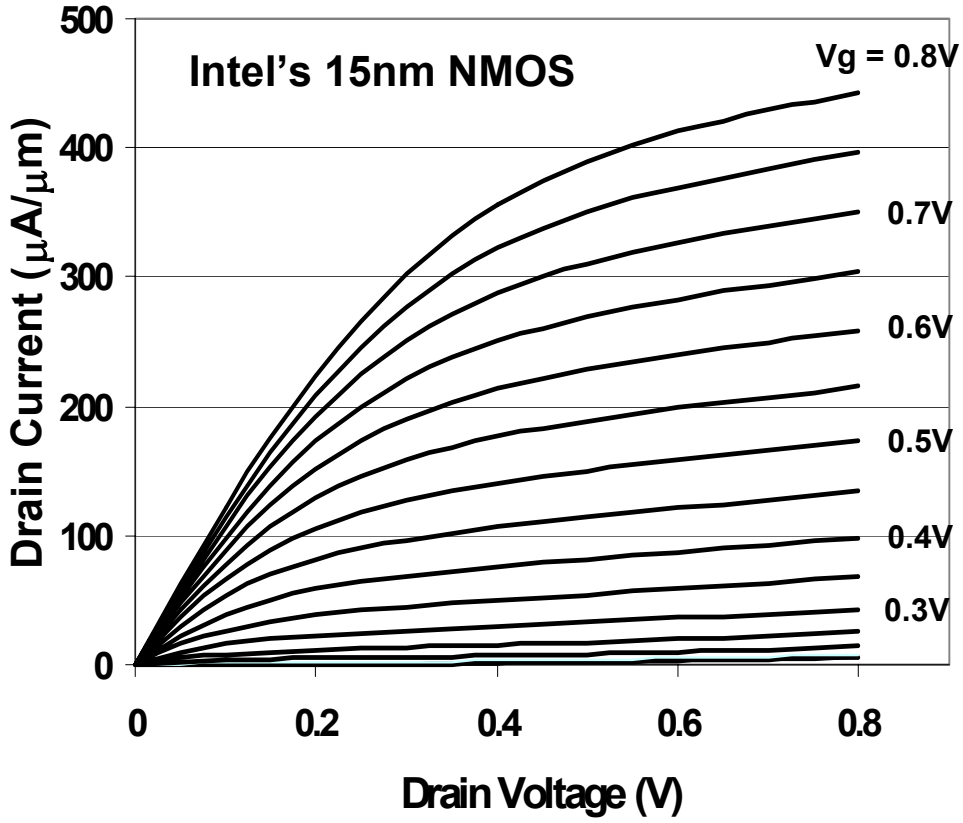
Intel's 20nm transistor
(June 2001)





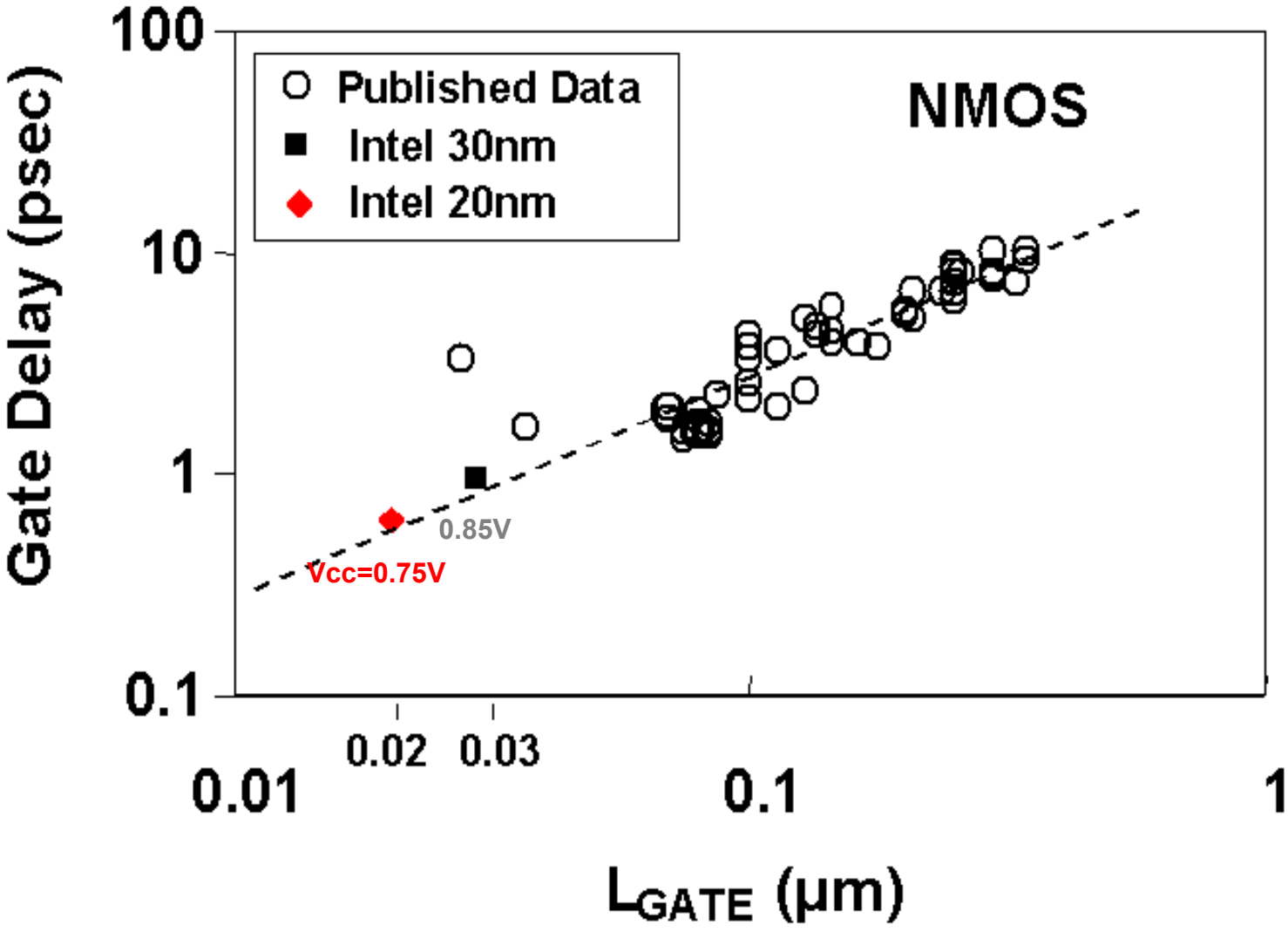
Intel's 15nm NMOS Transistor
(November 2001)



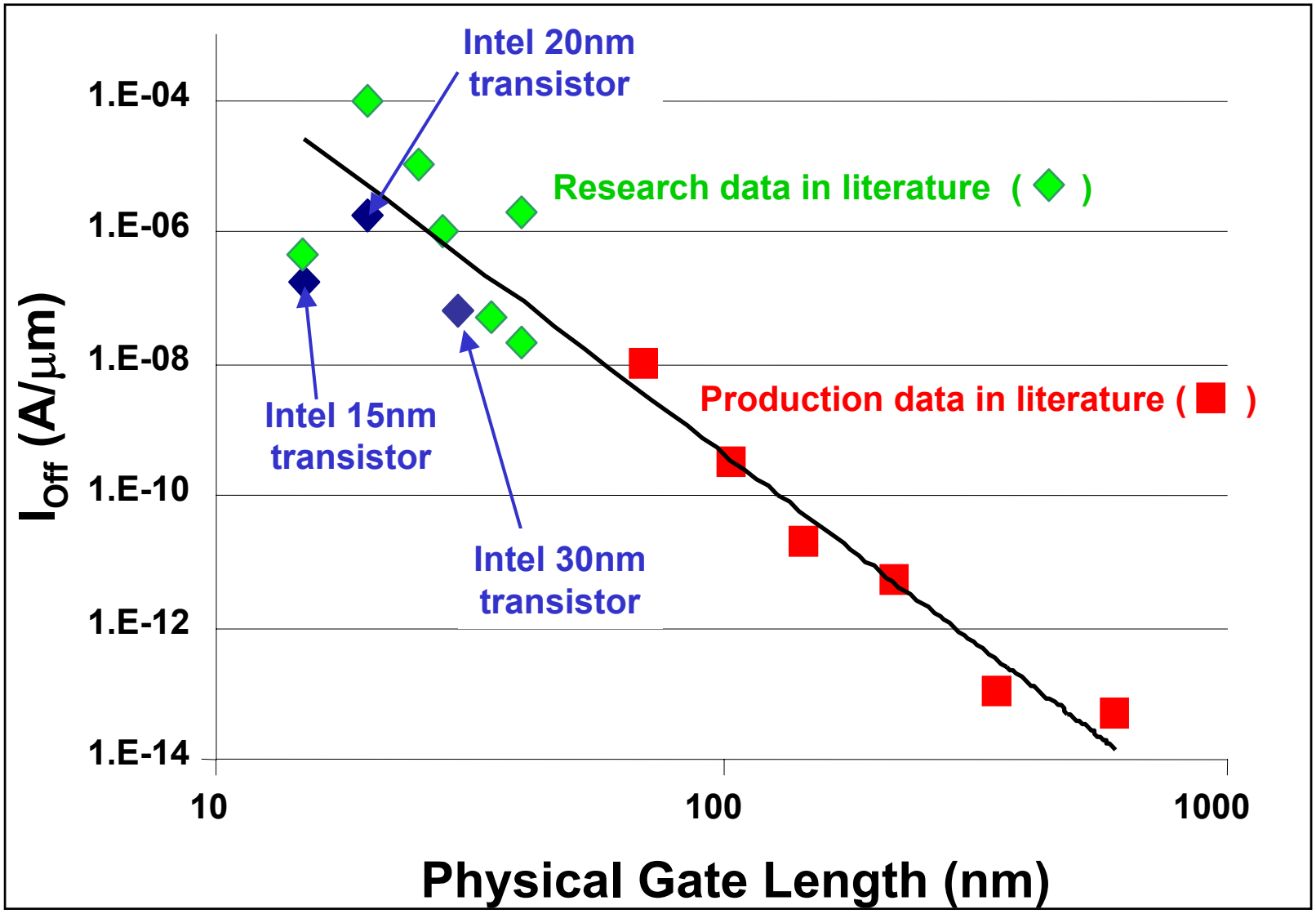


2.63 THz gate delay @ 0.8V!

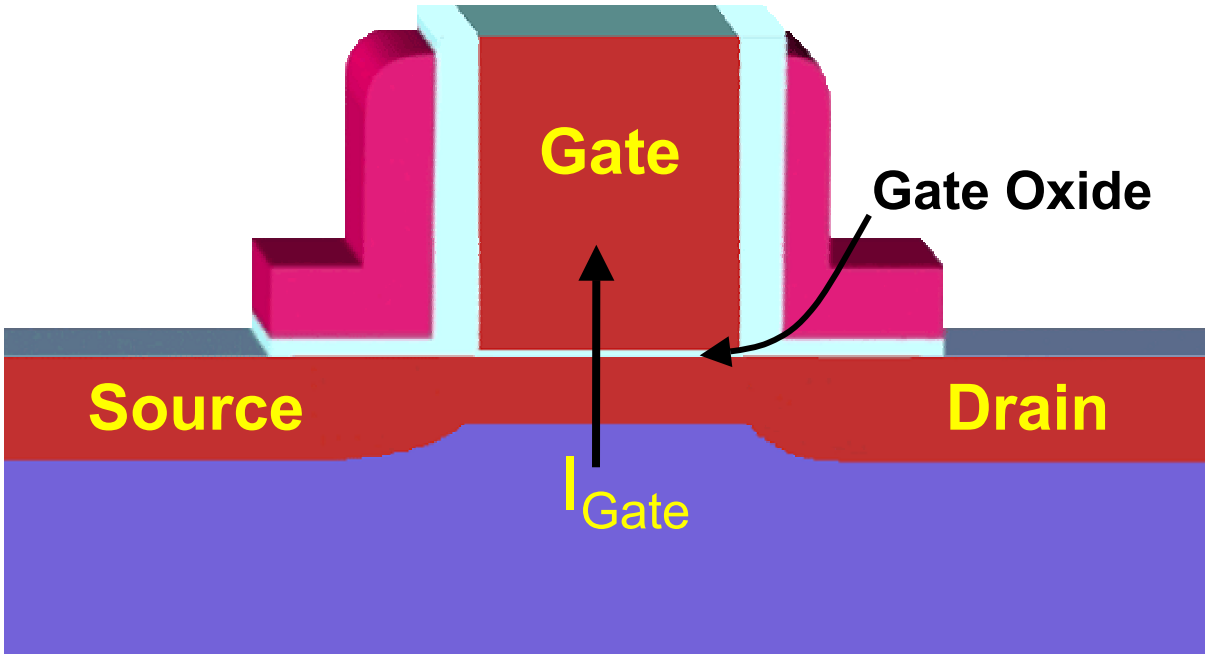
Gate Delay Trend Continues



….but I_{OFF} also Continues to Increase

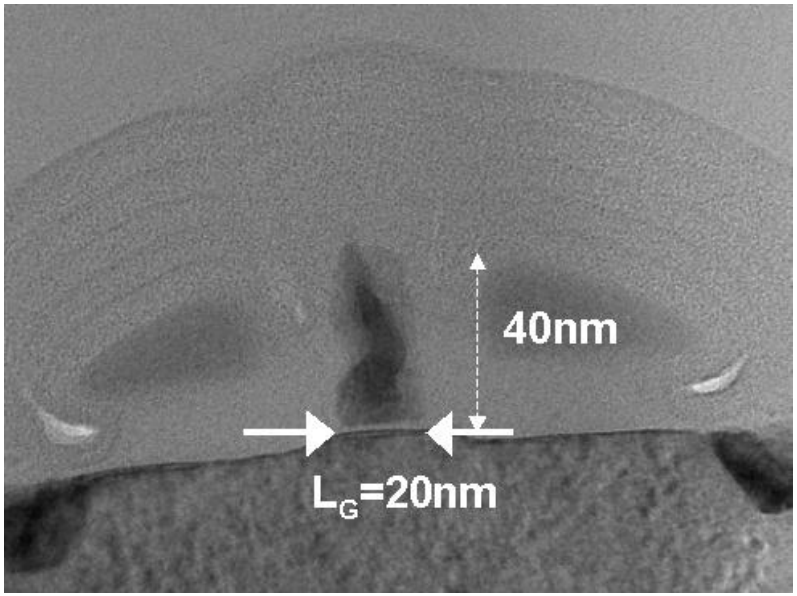


Challenges: Gate Leakage



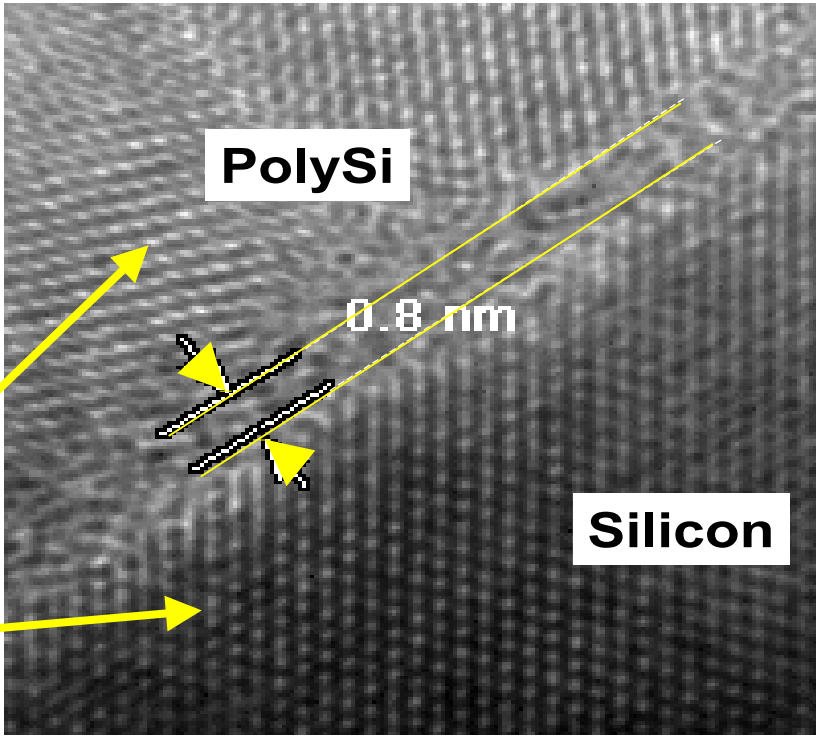
- **Gate Leakage Current**:
  - Thinner gate oxides produce faster transistors
  - We have reached the limit of Gate Oxide (SiO_2) scaling.
    - 30nm transistor had 0.8nm gate oxide
  - Thinner oxides leak more.
    - Gate oxide can get so thin it no longer acts as a good insulator.

Is There Any Oxide Left?



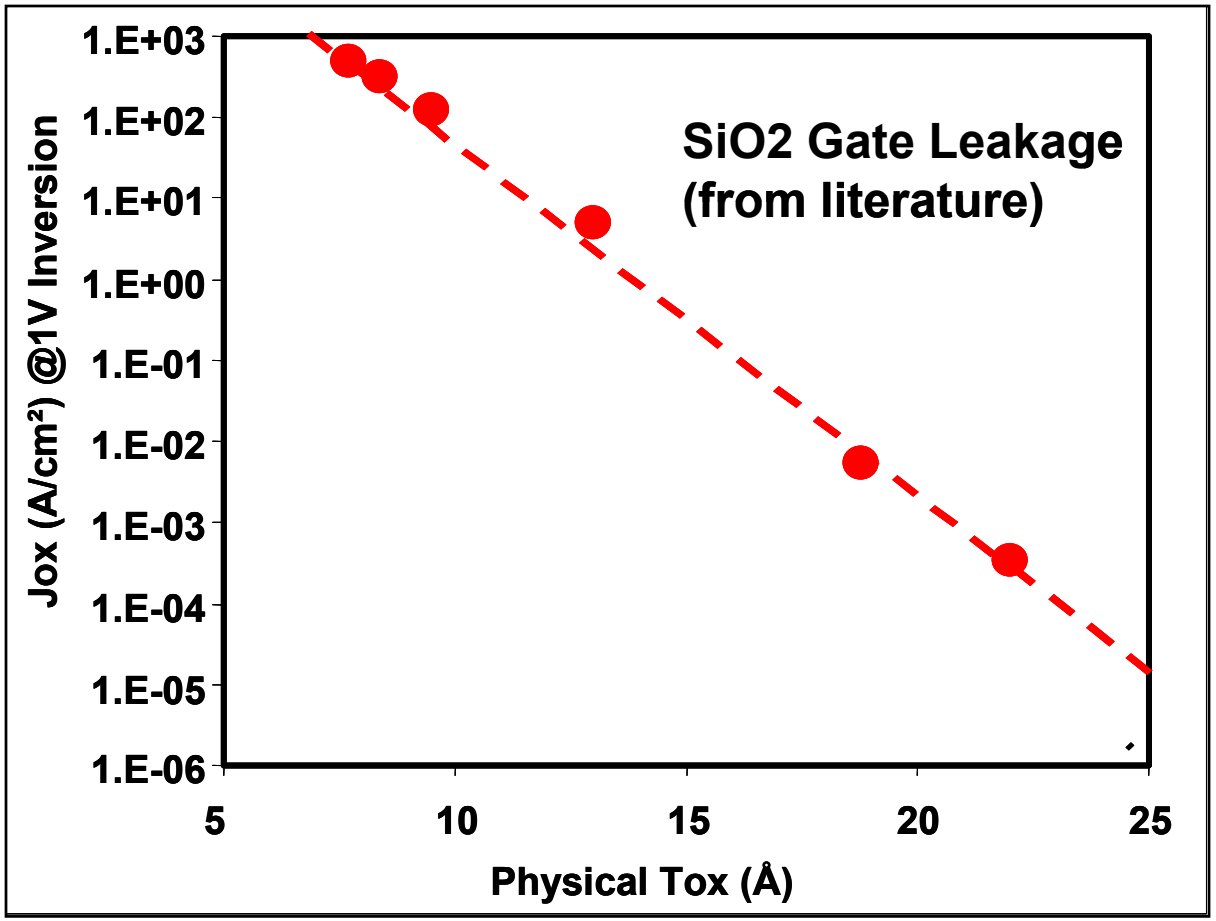
20 nanometer transistor

Gate oxide less than 3 atomic layers thick

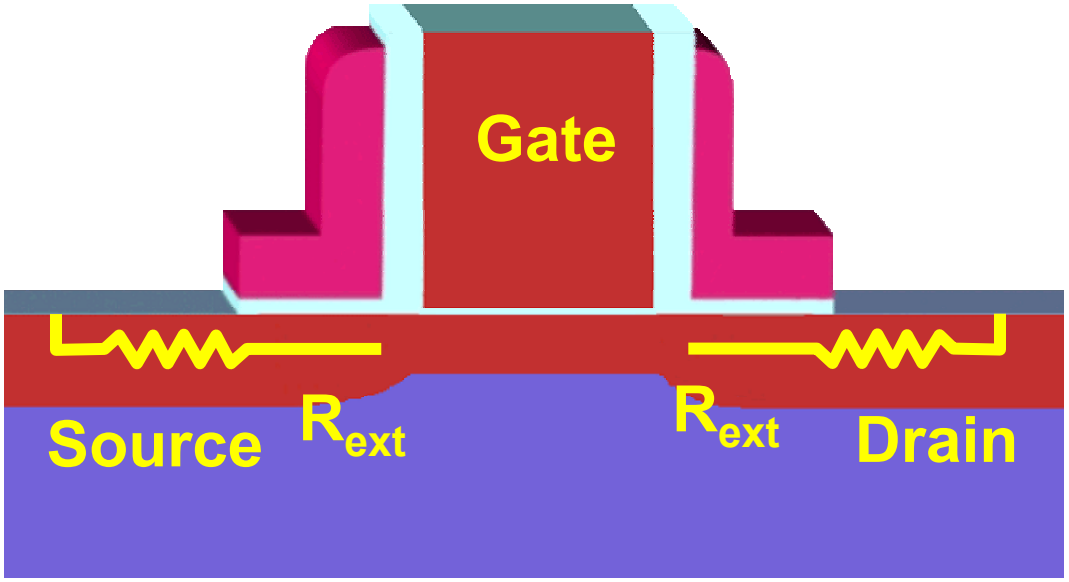


Atomic structures

….but Thin Gates have More Leakage

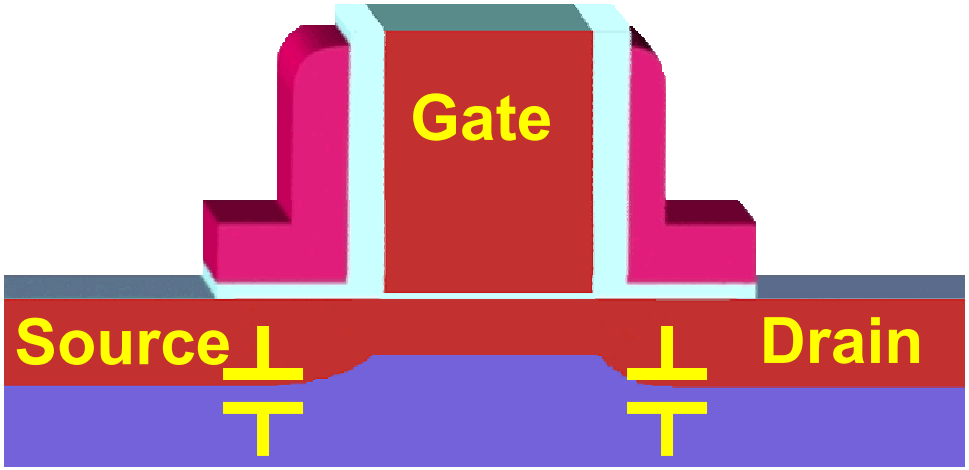


Resistance Challenges



- **Resistance: Challenges**
  - Thinner source and drains have more resistance.
  - Current “crowds” through thin source/drain regions.
  - Silicon doping density is at its saturation limit
  - We can’t lower the resistivity

Source/Drain Junction Capacitance



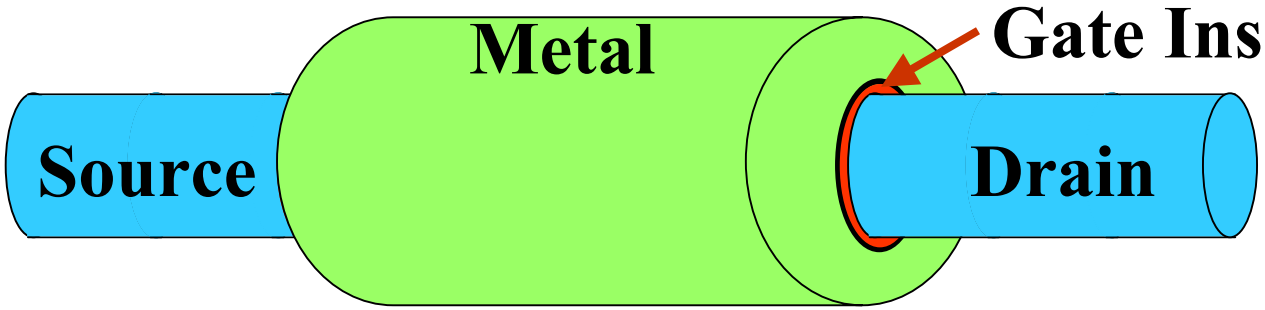
- **Capacitance**

A high source/drain junction capacitance takes longer for the transistor to build up enough energy to switch on and off.

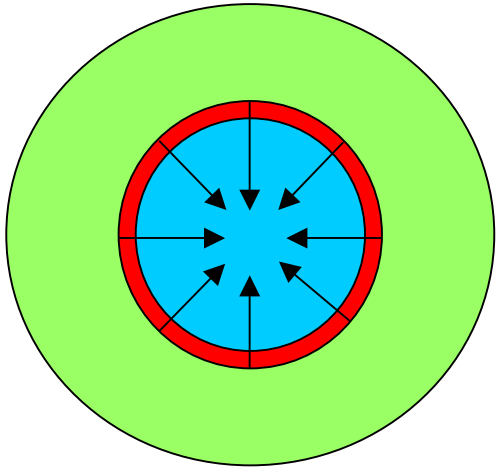
Agenda

- Solid State Physics Refresher
- MOS Device Physics Refresher
- Classical CMOS Limitations
- ***Non-classical CMOS***
- New Emerging Technologies
- Conclusions

The Ideal MOS Transistor



Fully Surrounding Metal Electrode



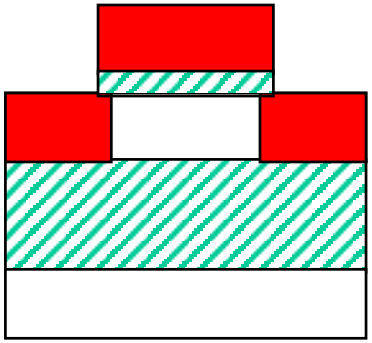
Fully Enclosed, Depleted Semiconductor

High-K Gate Insulator

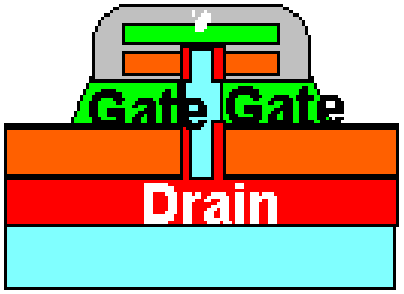
Band Engineered Semiconductor

Low Resistance Source/Drain

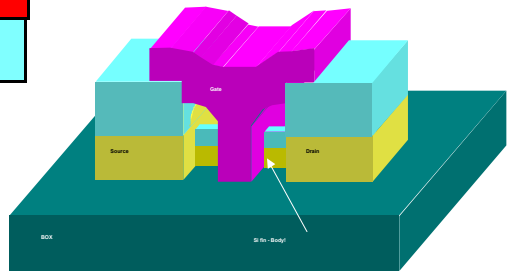
2001 ITRS
New Transistor Definitions

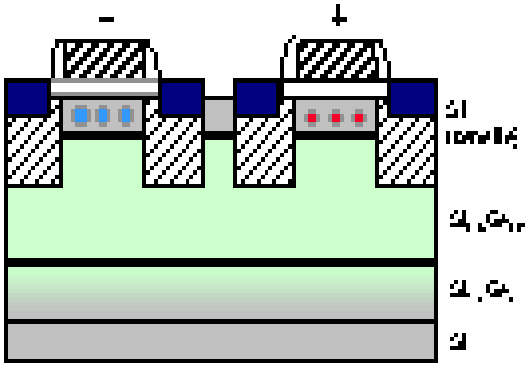


Ultra-Thin Body SOI

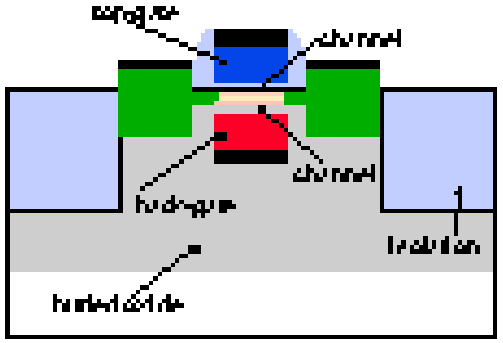


Vertical Tr



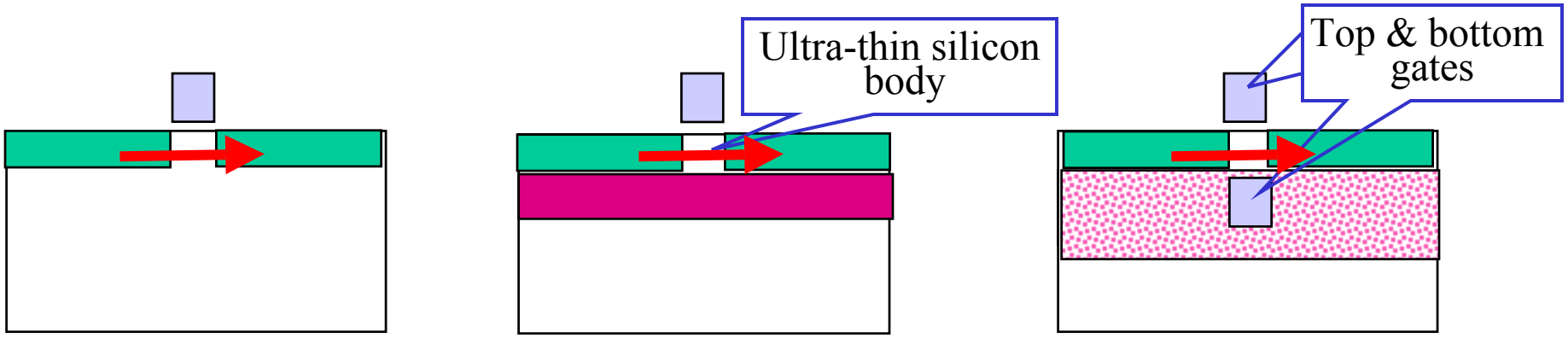


Band engineered Tr

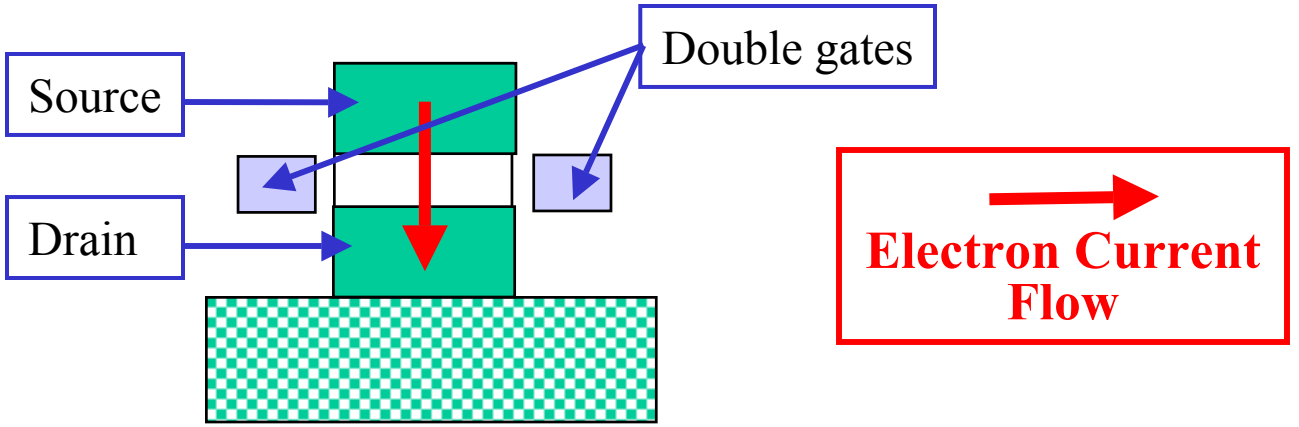


Double Gate Tr

Cross-sections of Non-Classical CMOS Devices

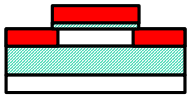
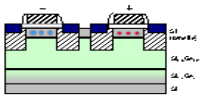
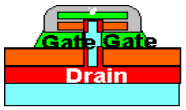
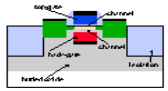


Bulk MOSFET **Ultra-Thin Body MOSFET** **Double-Gate MOSFET**

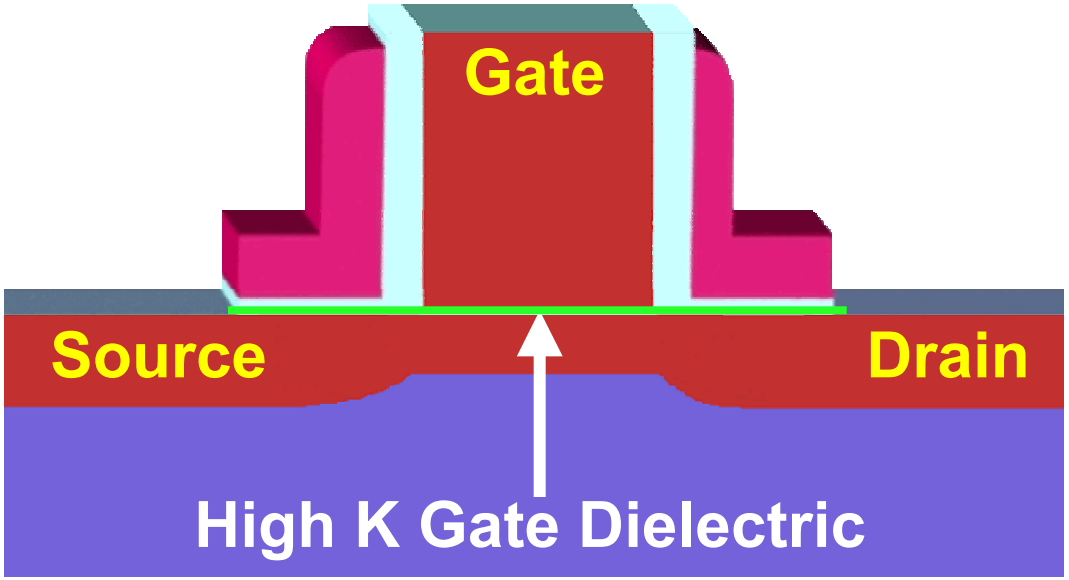


Vertical MOSFET

Non - Classical CMOS

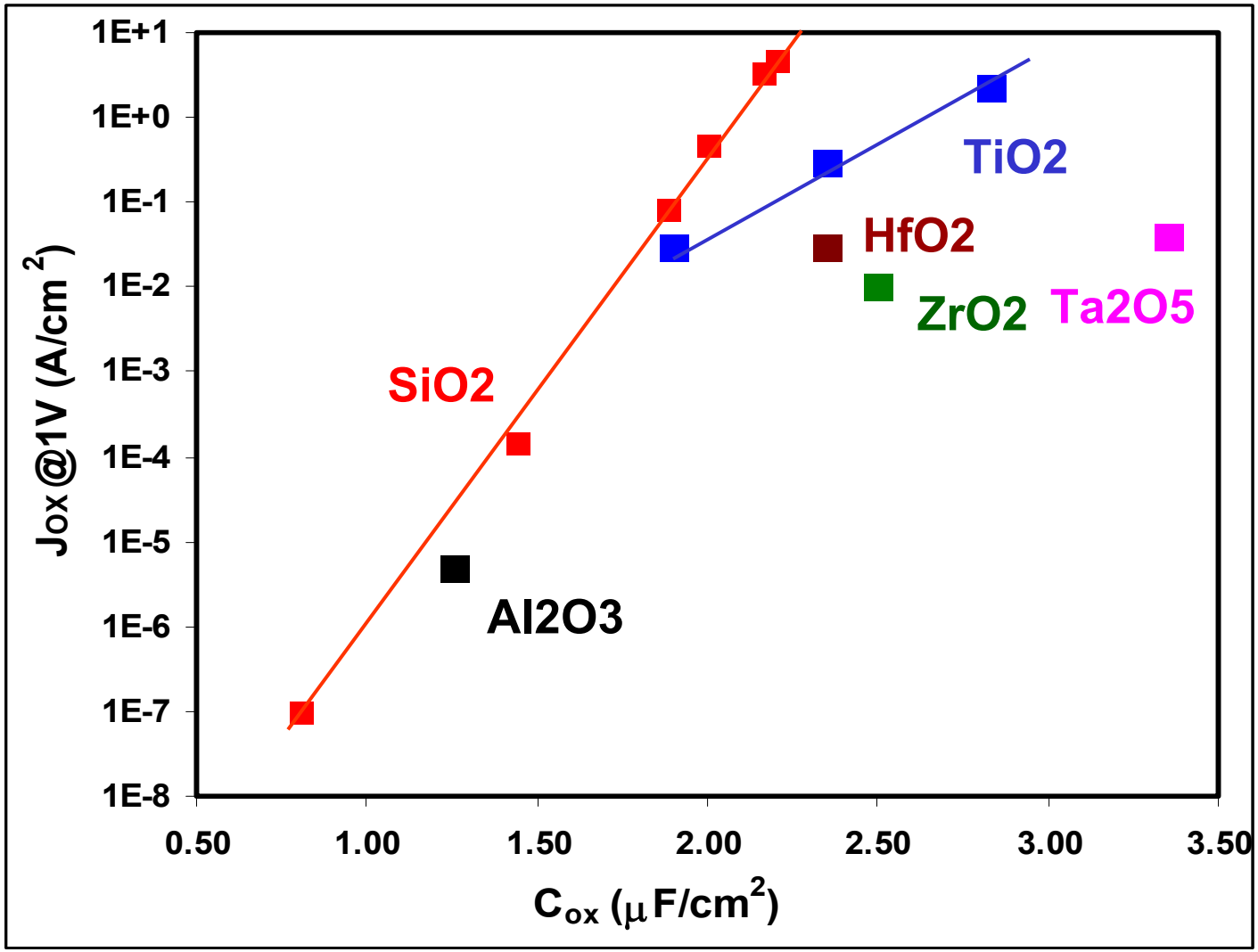
					
Device	*Ultra-Thin Body SOI*	*Band-Engineered Transistor*	*Vertical Transistor*	*FinFET*	*Double-Gate Transisto*
Concept	**Fully depleted SOI**	**SiGe or Strained Si channel; bulk Si or SOI**	**Double-gate or surround-gate structure (No specific temporal sequence for these three structures is intended)**		
Application/driver	**Higher performance, Higher transistor density, Lower power dissipation**				
Advantages	**-Improved subthreshold slope –V_t controllability**	**-Higher drive current -Compatible with bulk and SOI CMOS**	**-Higher drive current Lithography independent L_g**	**-Higher drive current -Improved subthreshold slope -Improved short channel effect -Stacked NAND**	**-Higher drive current -Improved subthreshold slope -Improved short channel effect -Stacked NAND**
Scaling Issues	**-Si film thickness -Gate stack -Worse short channel effect than bulk CMOS**	**-High mobility film thickness, in case of SOI -Gate stack -Integration**	**-Si film thickness -Gate stack -Integrability -Process complexity -Accurate TCAD including QM**	**-Si film thickness -Gate stack -Process complexity -Accurate TCAD including QM effect**	**-Gate alignment -Si film thickness -Gate stack -Integrability -Process complexity -Accurate TCAD including QM effect**
Design Challenges	**-Device characterization -Compact model and parameter extraction**	**-Device characterization**	**-Device characterization -PD versus FD -Compact model and parameter extraction -Applicability to mixed signal applications**		
Maturity	**Development**				
Timing	**Near Future** →				

High K Gate Dielectric

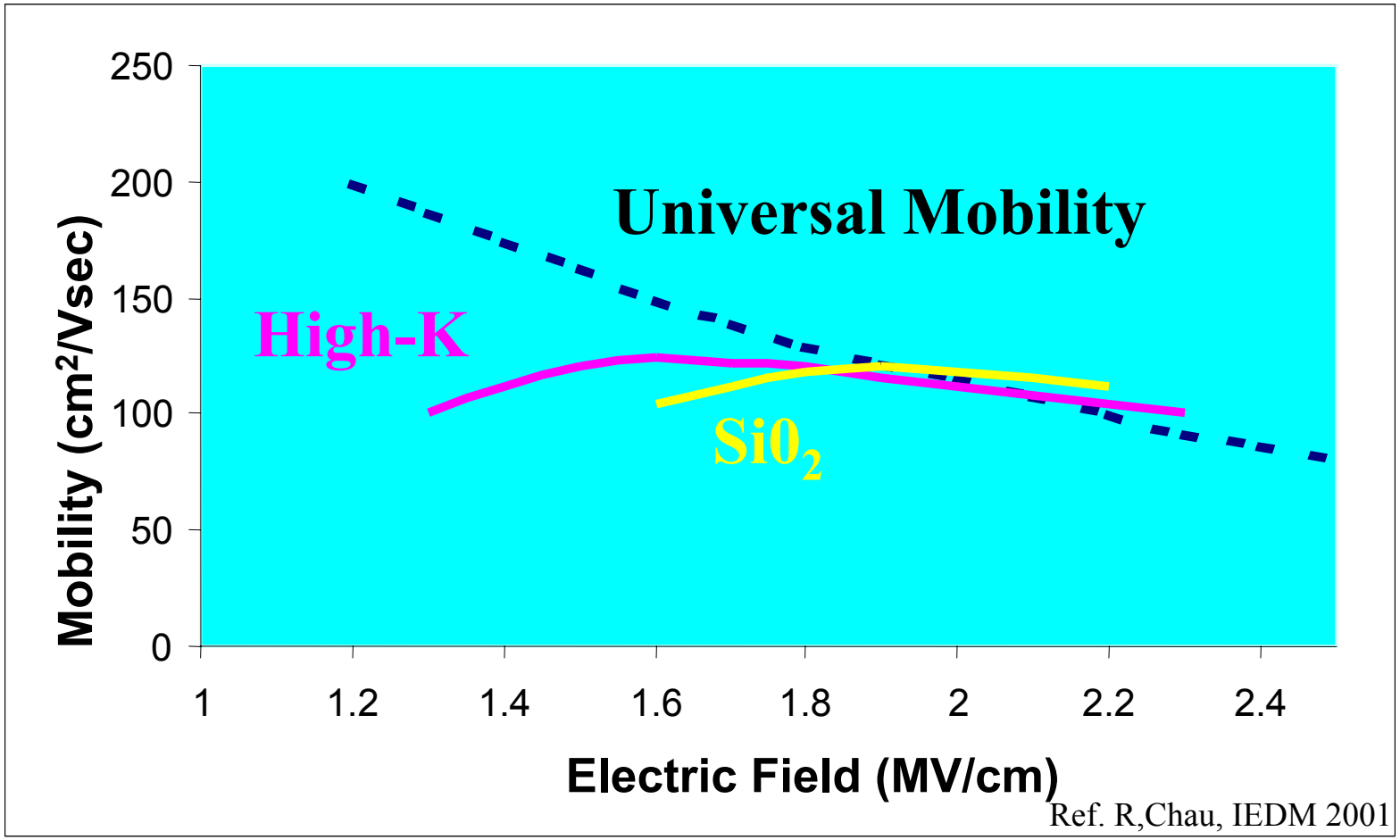


- **High K dielectric**
  - •New material replaces SiO_2
  - •Thicker physical film but same capacitance
  - •10,000x lower gate leakage current for same capacitance

Alternative Gate Dielectrics to Reduce Gate Leakage

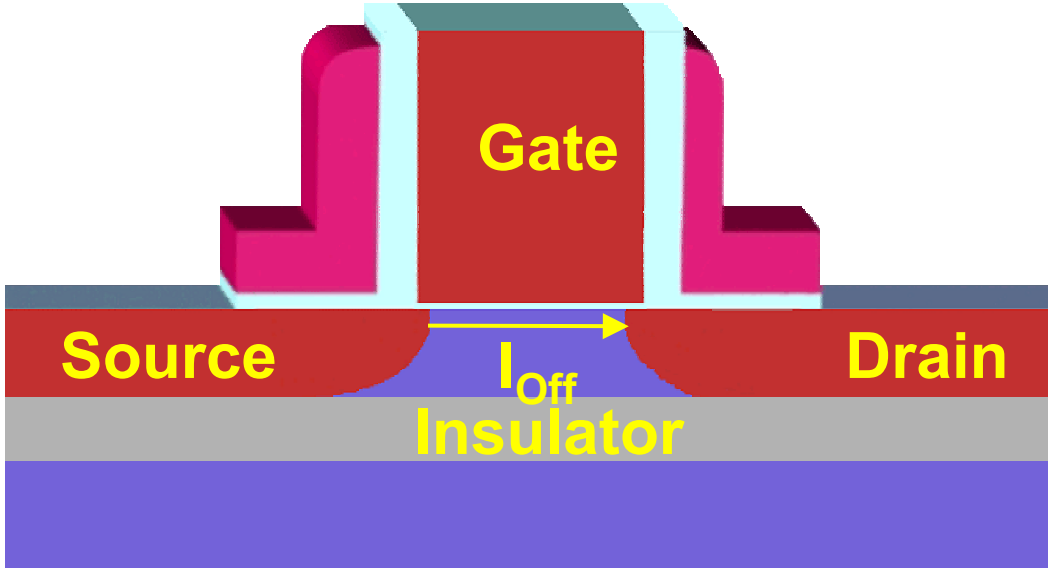


Comparable Effective Mobility for SiO_2 and High-K



Ref. R,Chau, IEDM 2001

Ultra Thin Body SOI



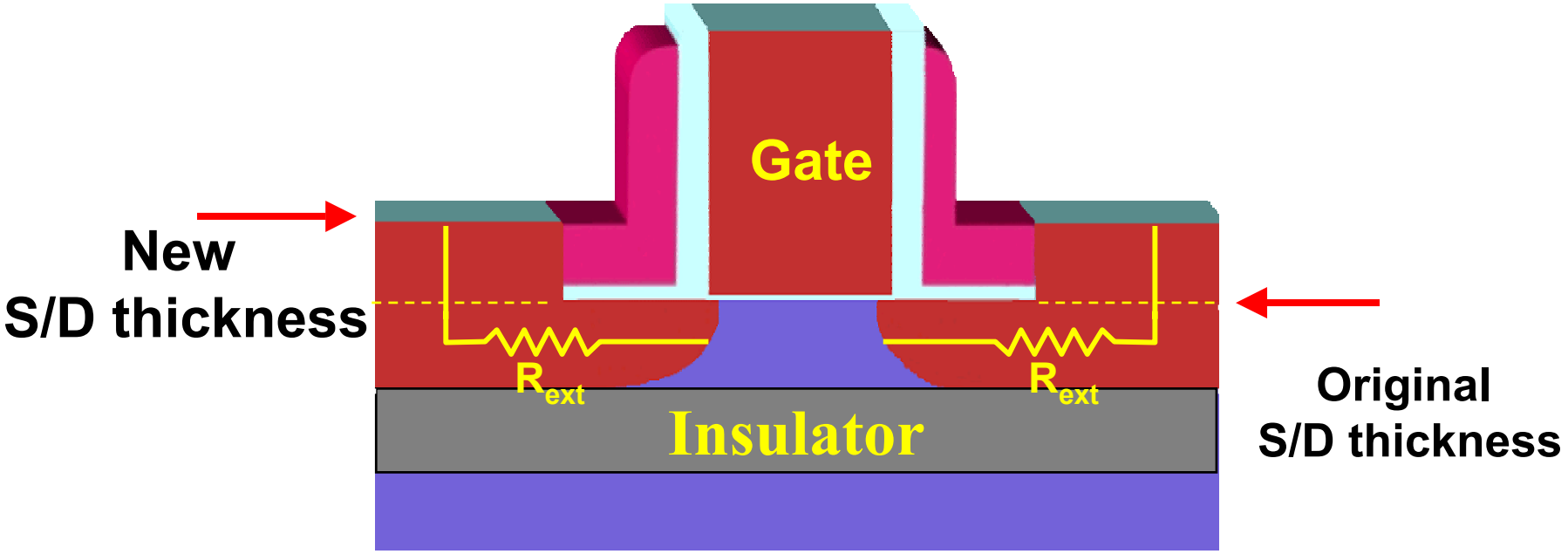
Benefits

- No leakage path through substrate
- Lowest junction capacitance
- Less voltage required to turn on transistor
- No floating body effect

Negative

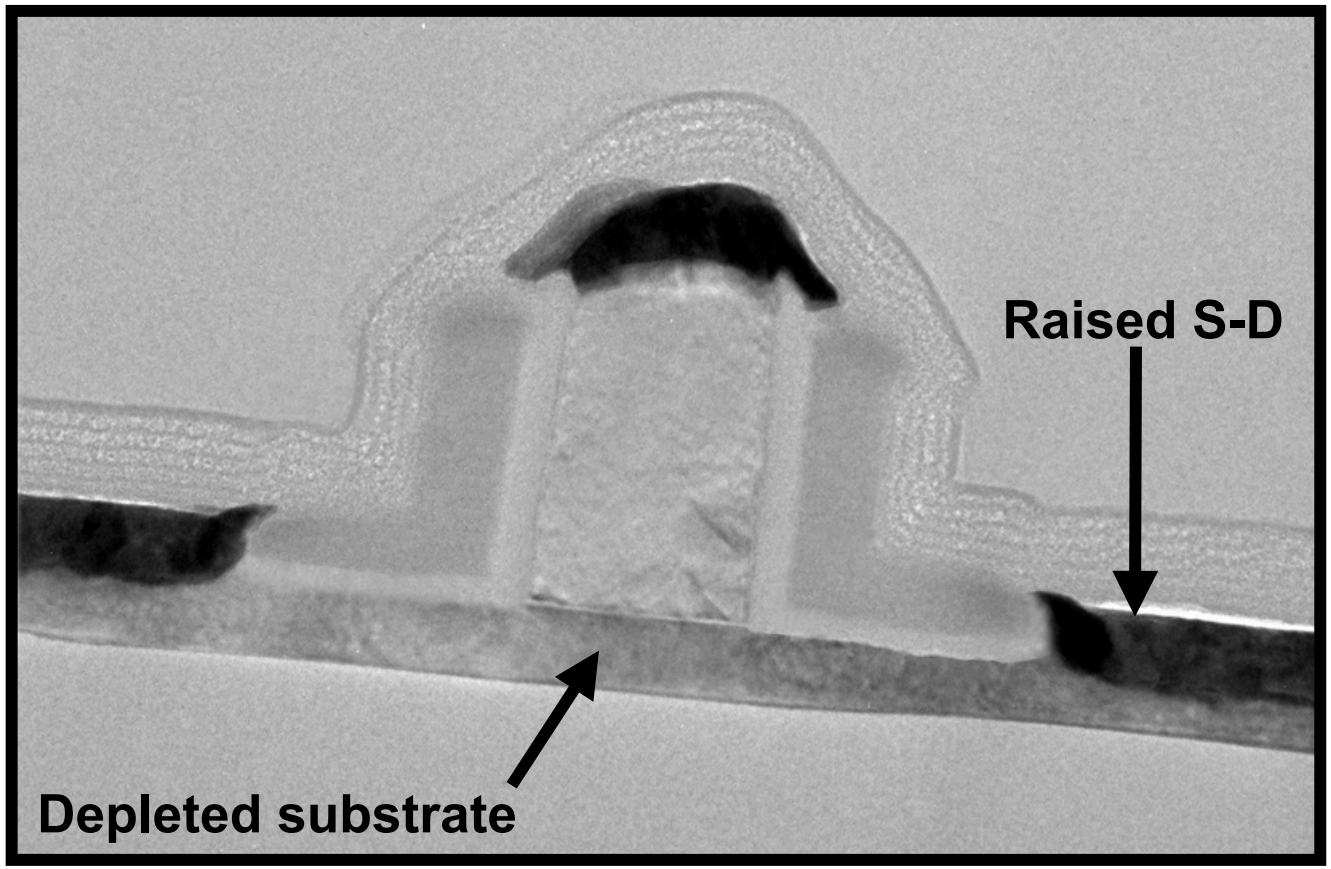
- High resistance in Source/Drains

Depleted Substrate Transistor

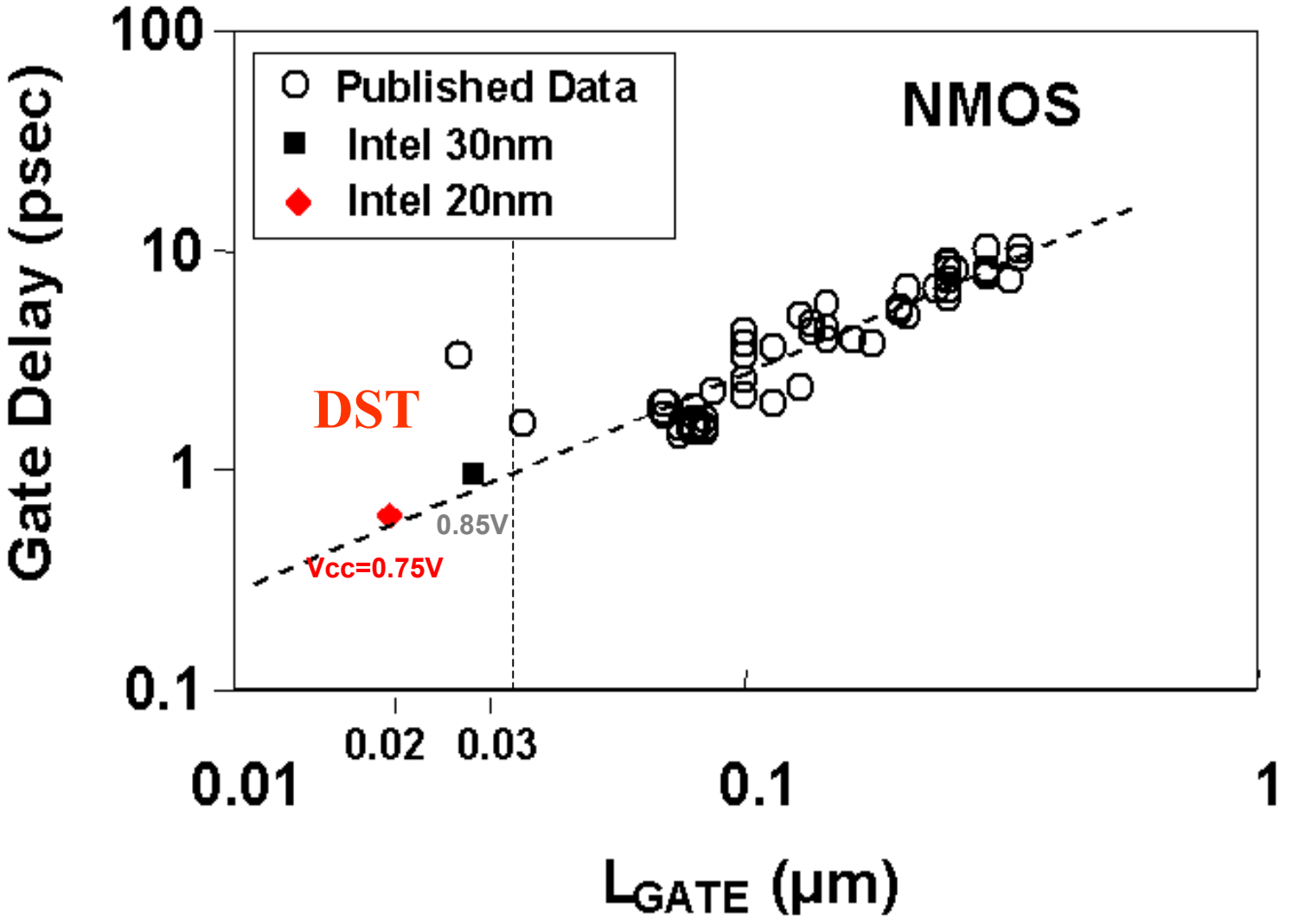


- **Ultra Thin SOI plus Epitaxy Grown Source Drain**
  - Decreases resistance
  - Higher drive current
  - No increase in junction capacitance

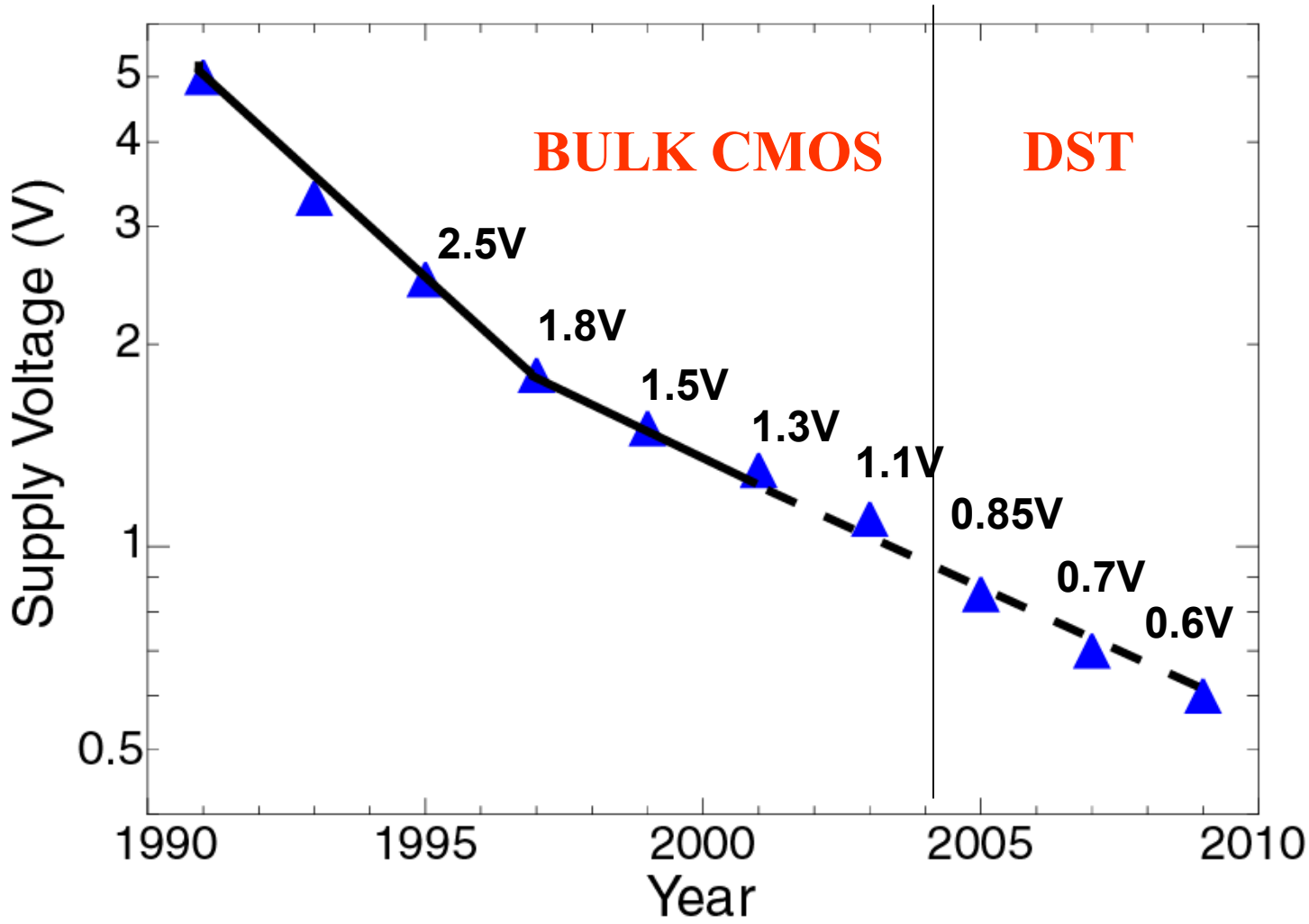
Raised Source-Drains Combined with Depleted Substrate



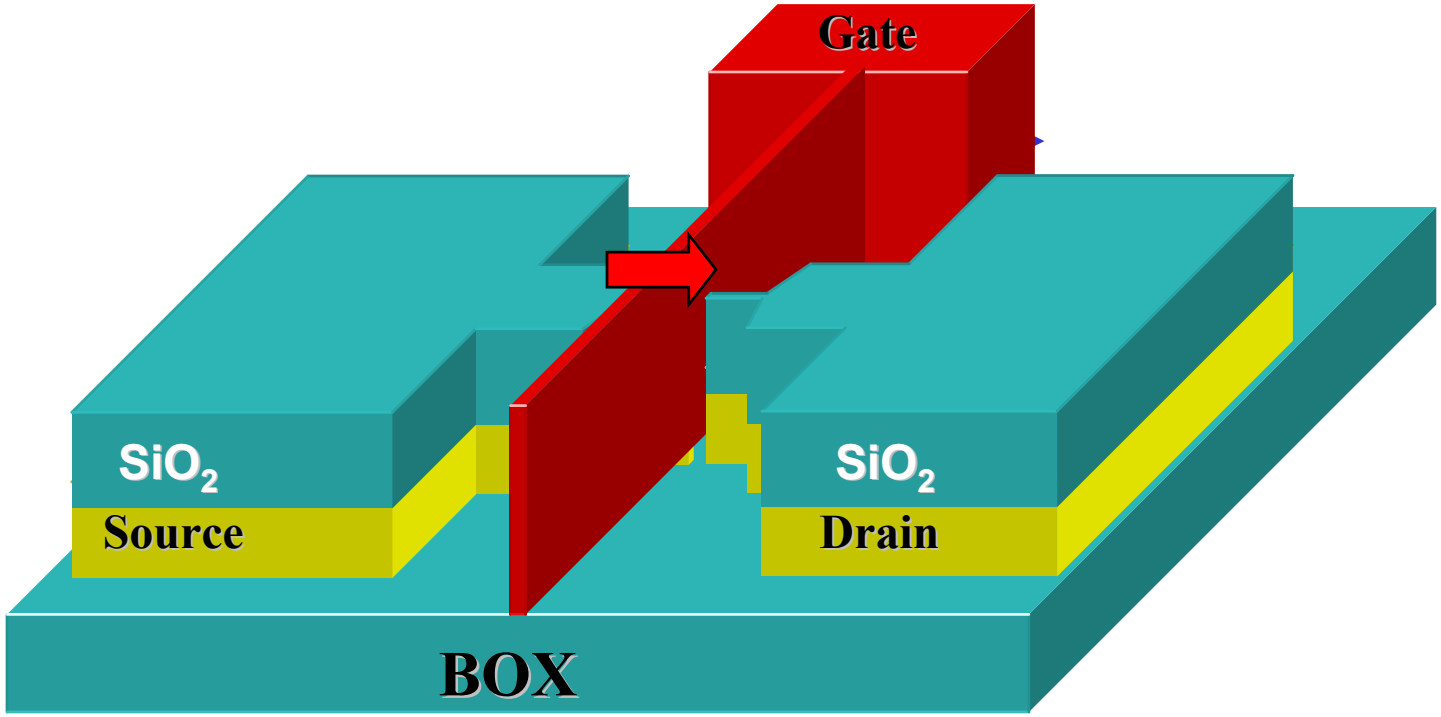
Gate Delay Trend Continues



DST Enables Future Voltage Scaling



Cross-sections of Non-Classical CMOS Devices



FinFET

How Small is Small?

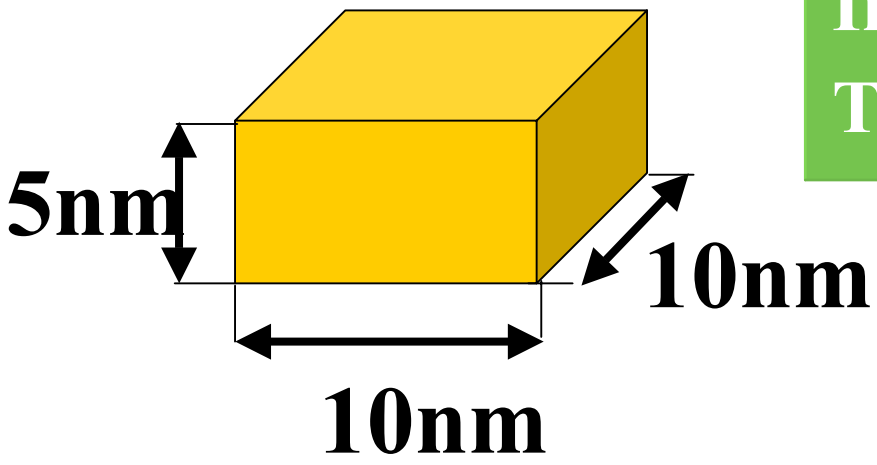
- ***Ultra Thin Body SOI (UTBSOI)***
  - Fully Depleted transistors have been demonstrated with Lg=25nm (Tsoi=6nm)
  - Simulations from University of California Berkeley show that UTBSOI can be scaled to Lg=12nm
  - Rule of thumb: Minimum Lg~2Tsoi
- ***Fin FET***
  - Good performance of FinFET demonstrated for sub-20nm Lg (W_{FIN}~10nm)
- Scalability of other ***multi-gate*** transistor structures reported

Can You Count the Atoms?

Silicon Atoms/cm^3= $5x10^{22}$

Volume=(10x10x5)nm^3=500 nm^3 1cm=10^{-7}nm

Number of atoms=($5x10^{22}x500x\ 10^{-21}$)=25000



Implanted Atoms/cm^3=(10^{19})

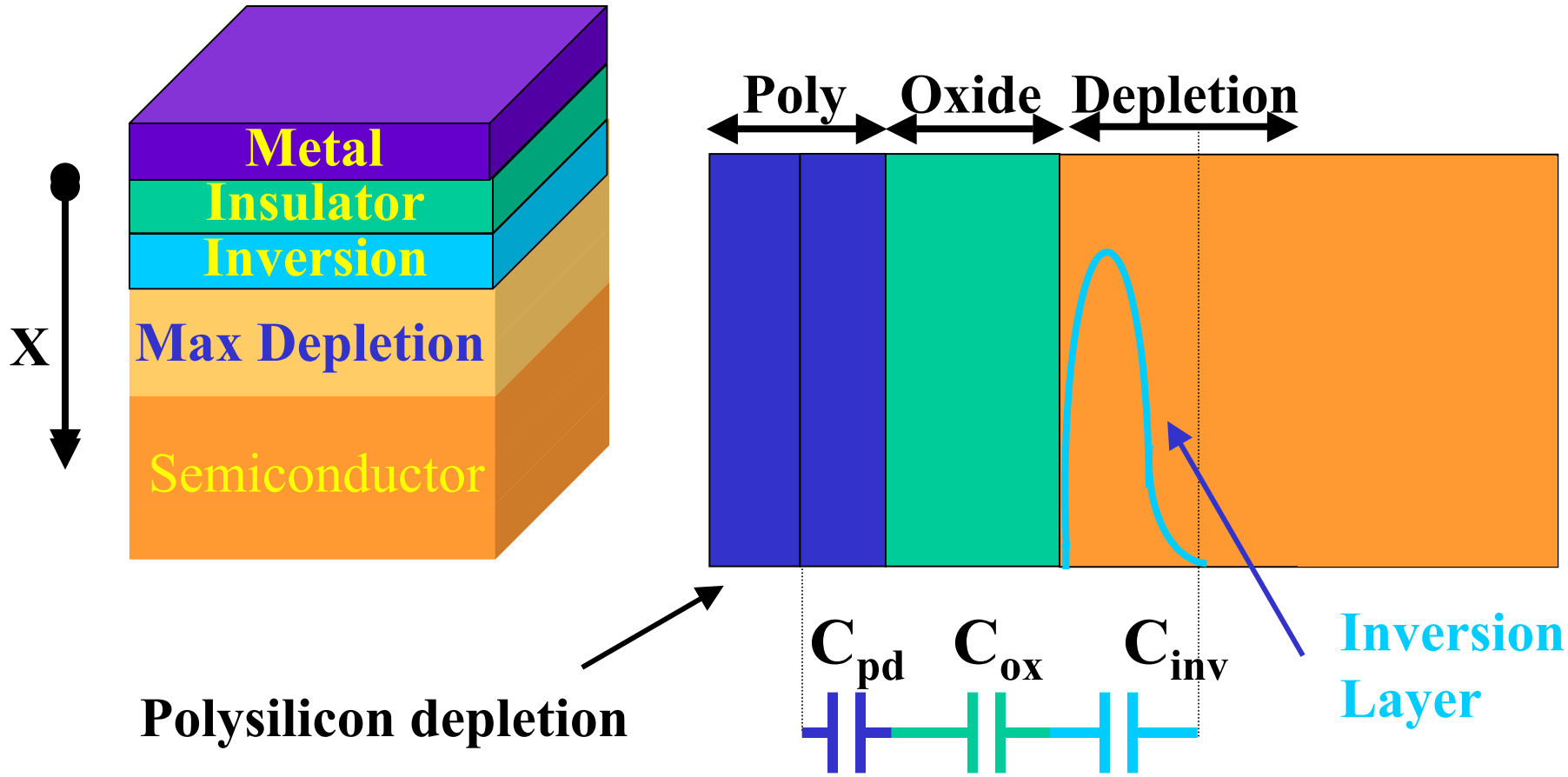
Total number of atoms=5

Threshold Voltage Must Be Adjusted Via Φ_{MS}

Agenda

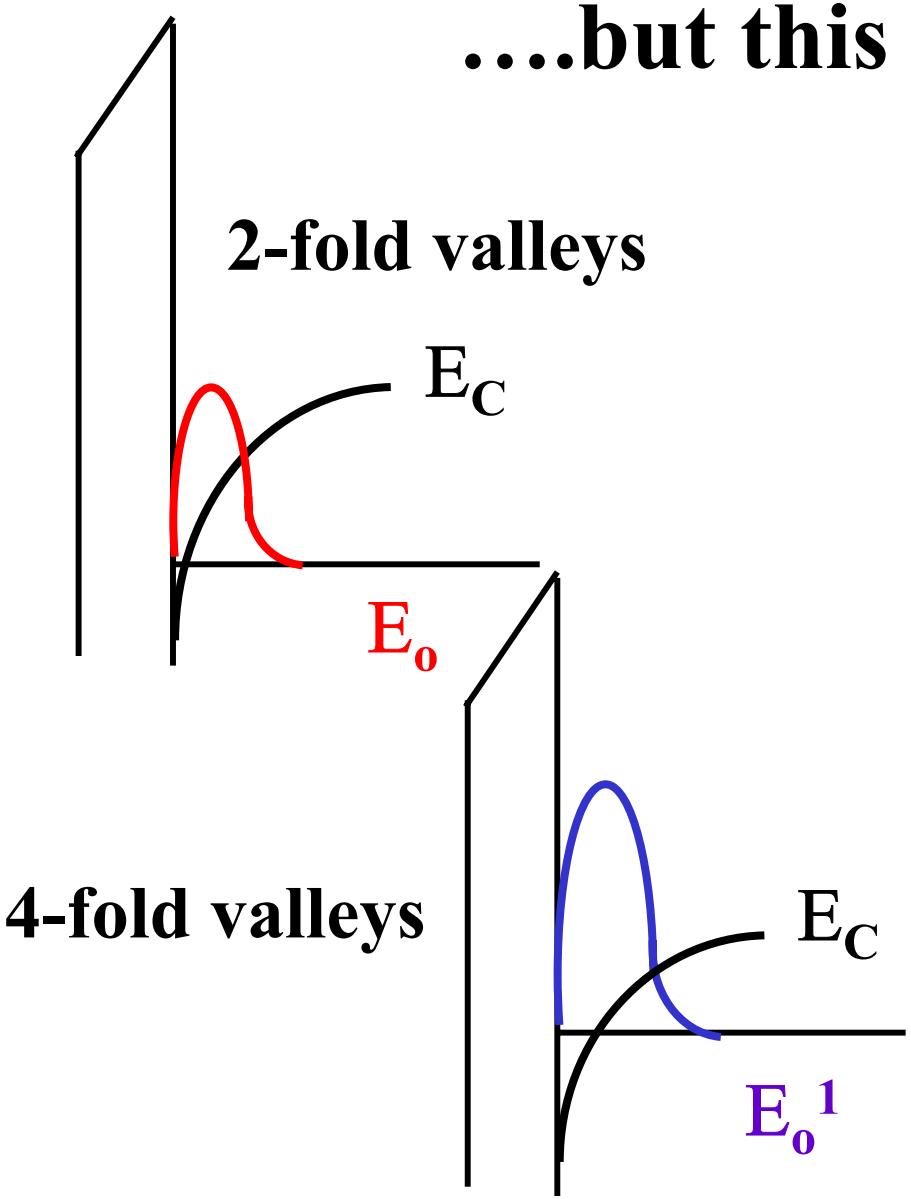
- Solid State Physics Refresher
- MOS Device Physics Refresher
- Classical CMOS Limitations
- ***Non-classical CMOS***
  - ***Quantum Effects***
- New Emerging Technologies
- Conclusions

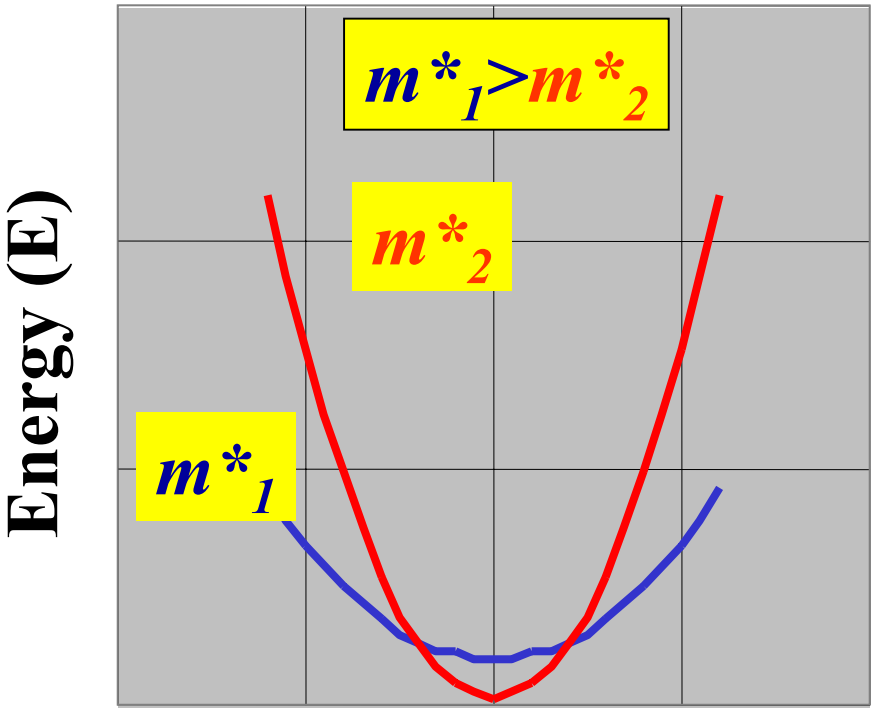
Capacitance Reduction



=>Metal Gate is needed to eliminate polysilicon depletion

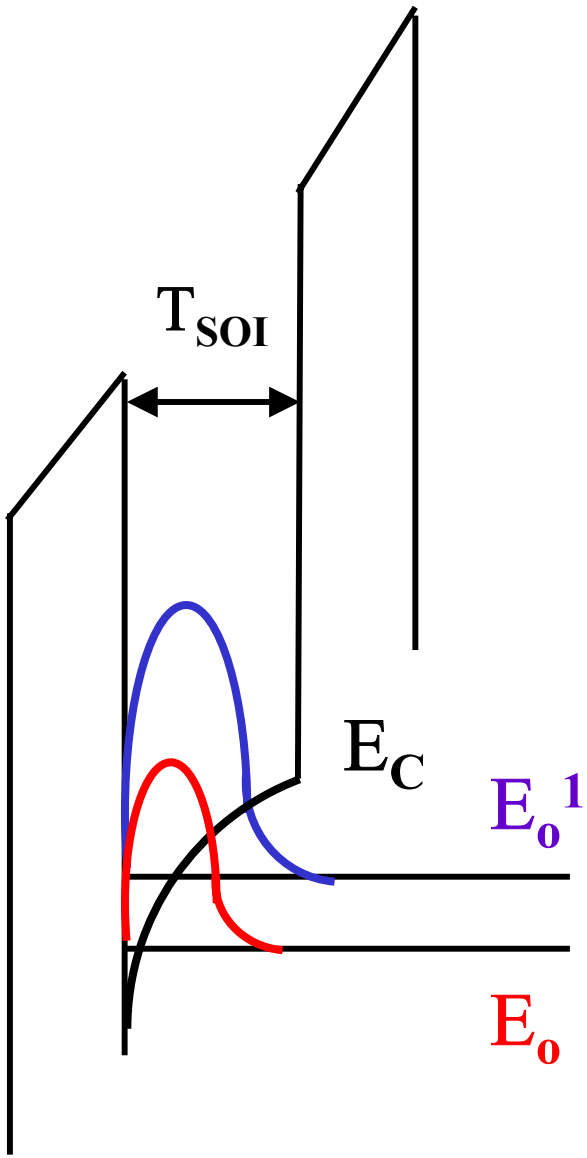
….but this is not all there is!

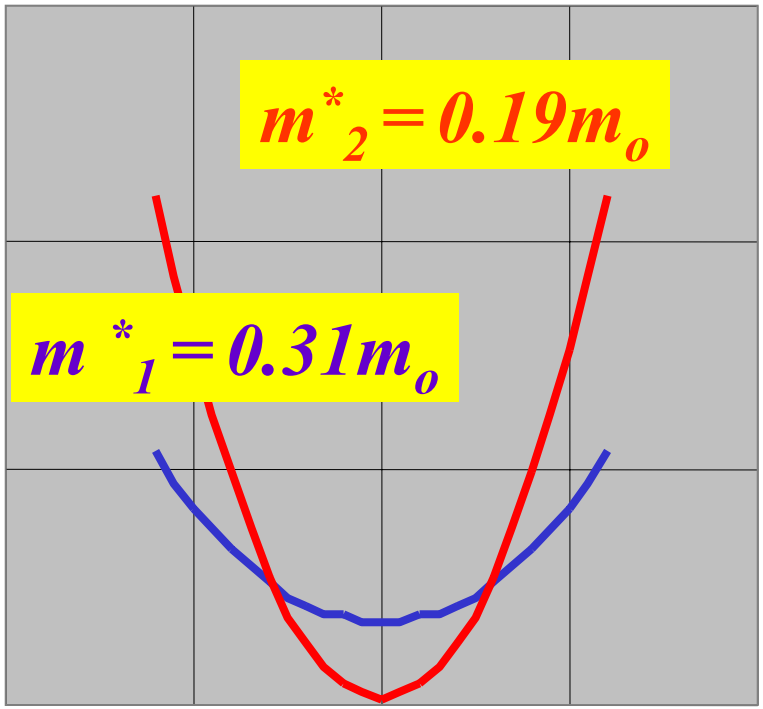




Light m* means higher μ => faster transistors

Sub-Band Engineering: Effect of Thickness (T_{SOI})

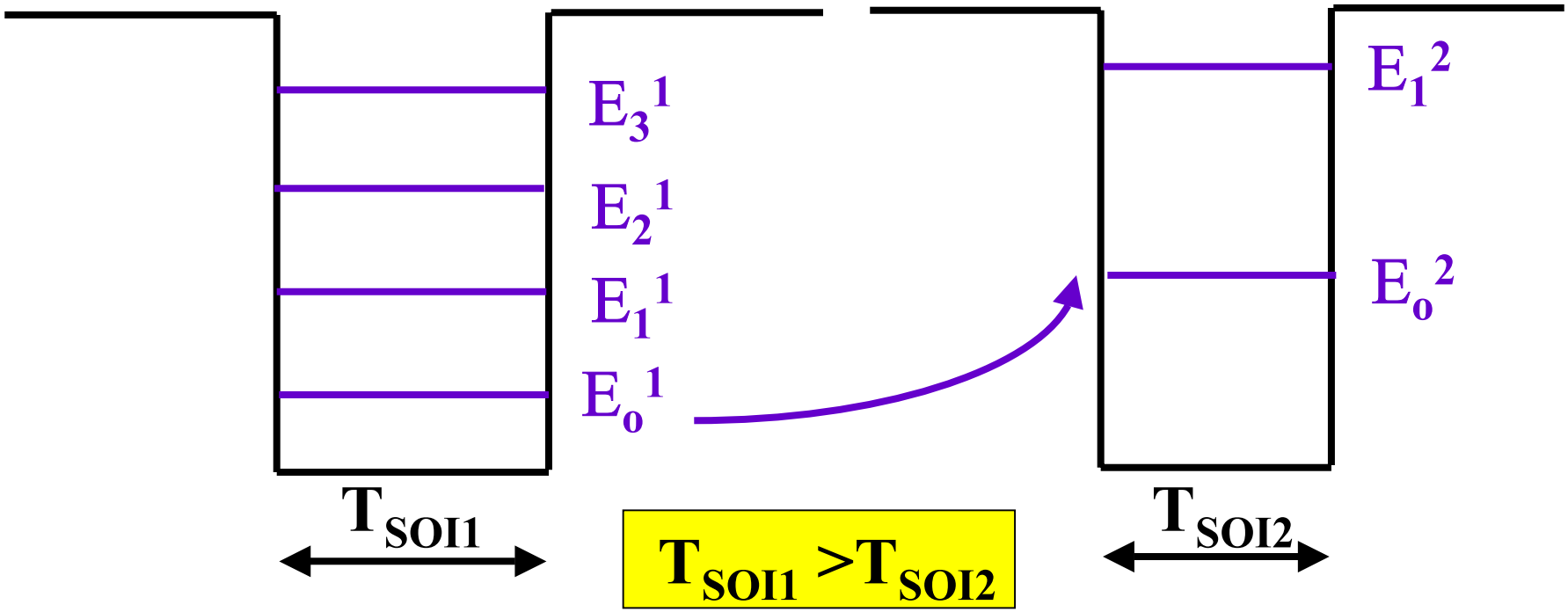




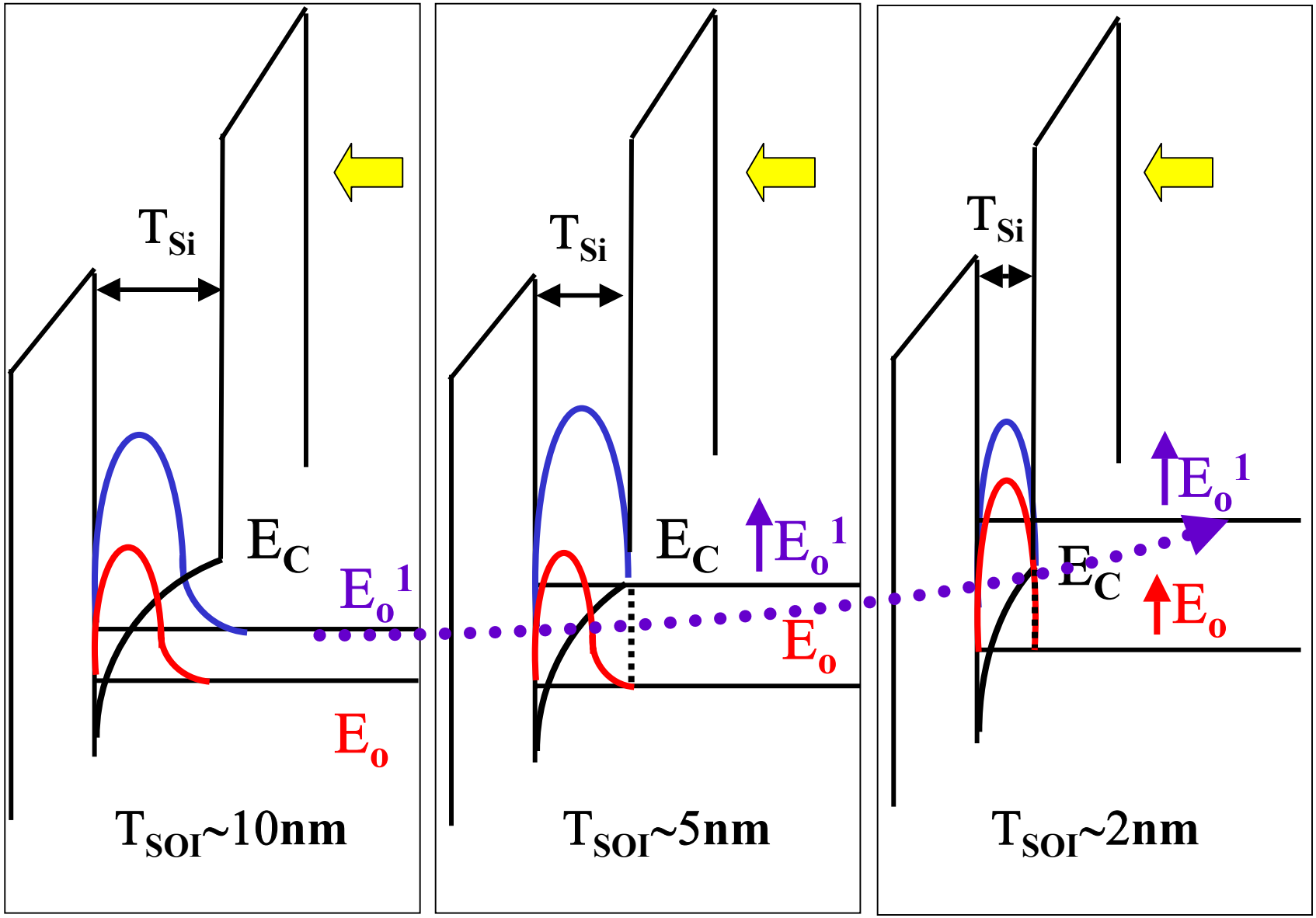
$\Delta E = E_o^1 - E_o$

E^1o Increases as the Well Width Decreases

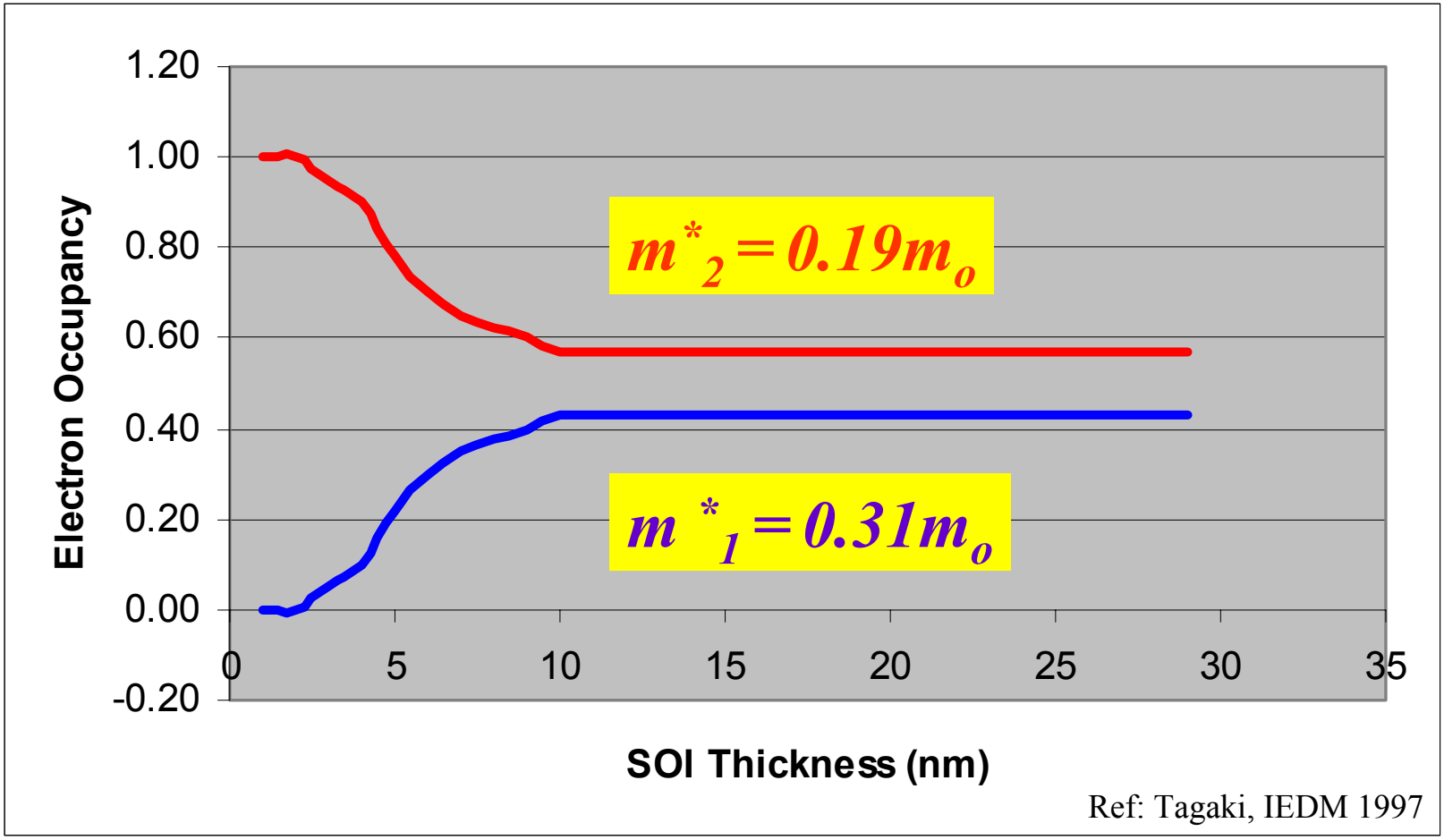
$$E_n = (\hbar^2 / 2m^*) (\pi / T_{SOI})^2 n$$



Effect of T_{SOI} on Sub-Band Occupation

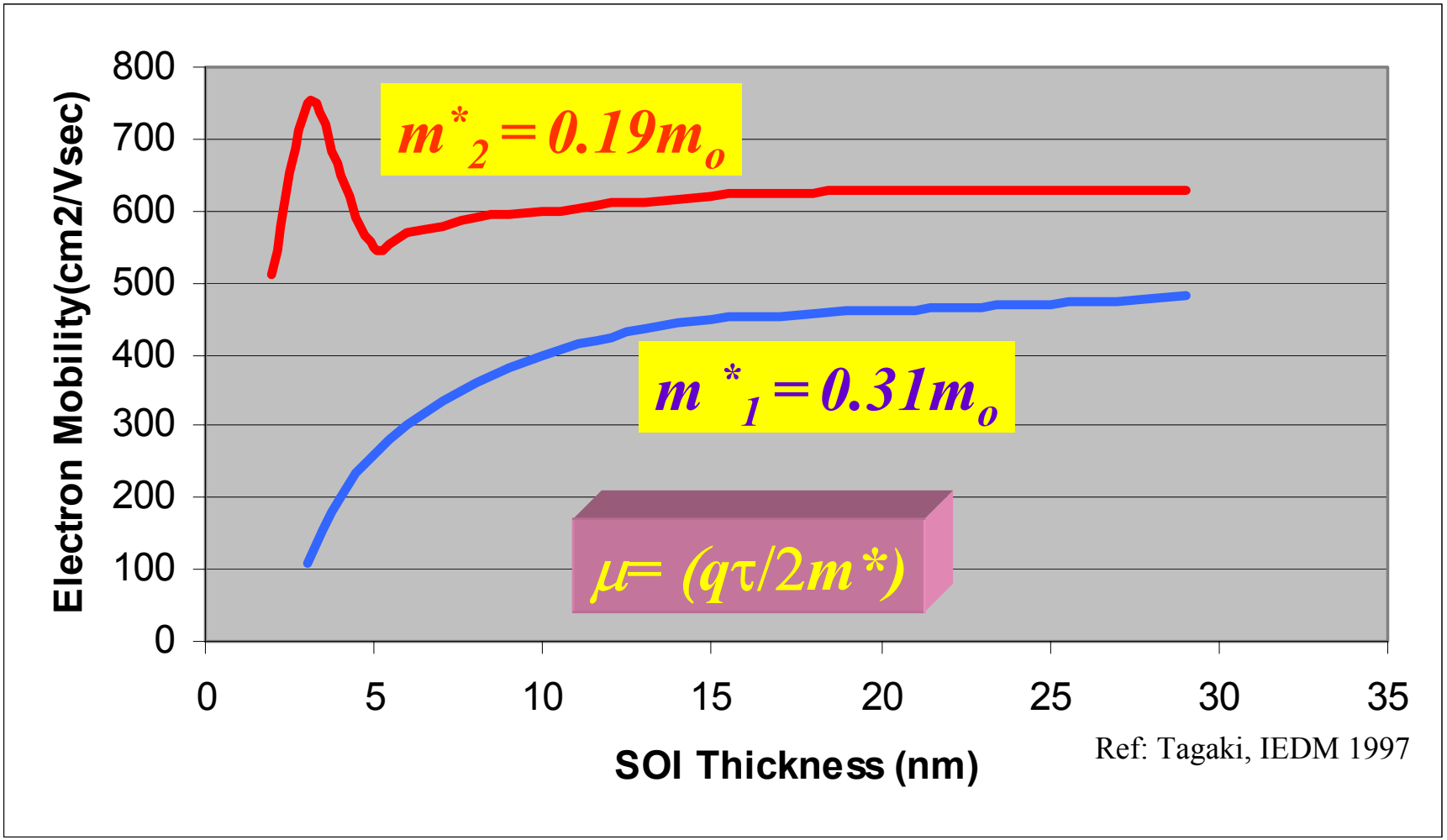


Electron Occupancy in Different Sub-Bands



Ref: Tagaki, IEDM 1997

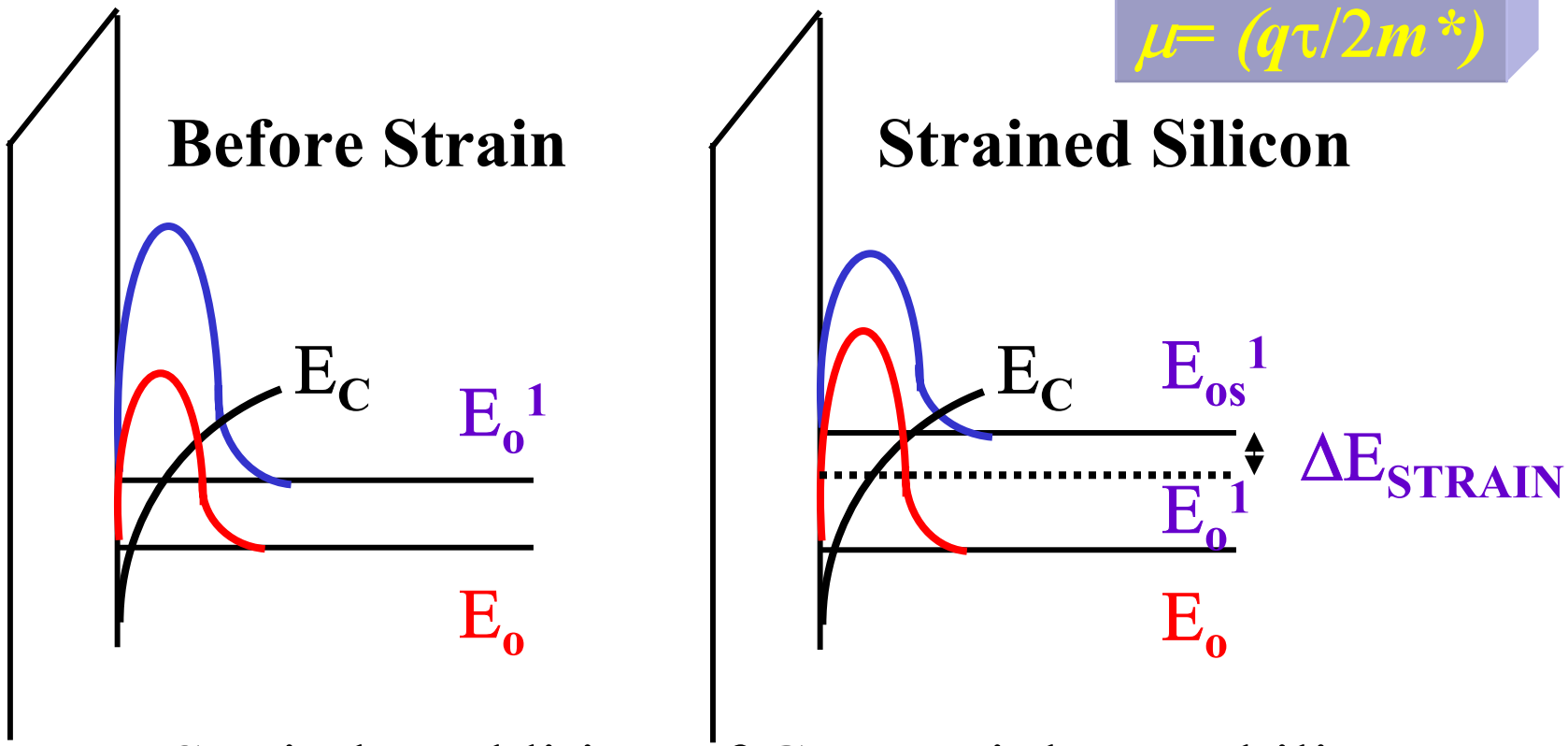
Mobility of Electrons in Different Sub-Bands



Sub-Band Engineering: Effect of Strain

$$\Delta E = \Delta E_{STRAIN} + (E_o^1 - E_o)$$

$$\mu = (q\tau/2m^*)$$



E.g.:Strain by addition of Ge=> Higher mobility

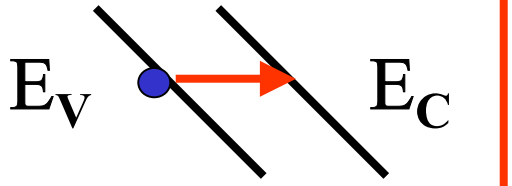
What is The Next Limit?

Band to Band Tunneling

$E_{max} > E_{usable} \sim 5 \times 10^5$ V/cm 1cm=10^{-7}nm

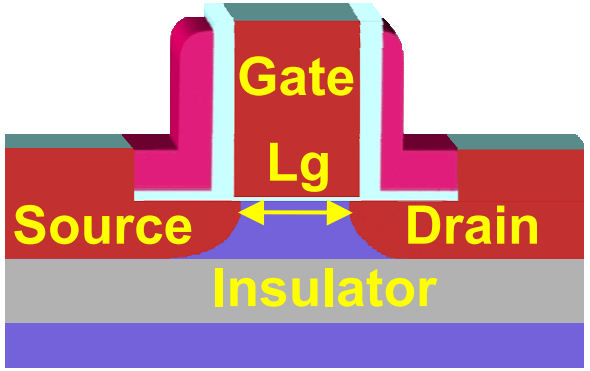
$E_{usable} \sim 5 \times 10^5 \times 10^{-7}$V/nm=$5 \times 10^{-2}$V/nm

10^6 V/cm $> E_{max}$



Band to Band

$E_{usable} \sim$500mV/10nm



Lg=10nm

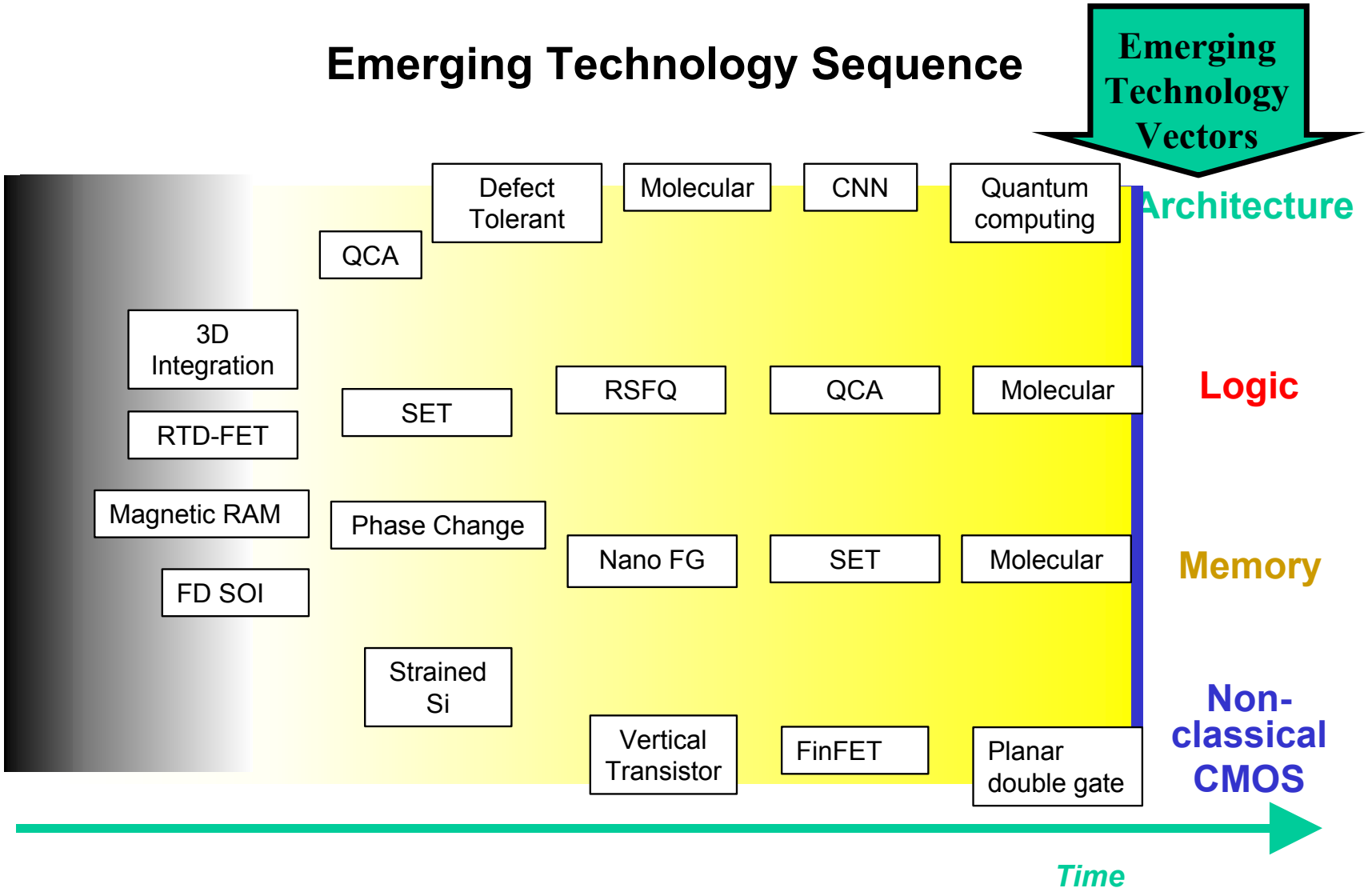
Summary of Quantum Effects in Silicon

- Conduction Band consists of multiple sub-bands
  - Lower energy sub-band has smaller m*=>higher μ
  - Higher energy sub-band has larger m*=>lower μ
- Reducing UTBSOI thickness below10nm splits the energy sub-bands further apart
  - Higher occupancy of lower m* band =>higher μ
  - Smaller width of inversion layer=> higher C_{inv}
- Straining silicon (e.g., by means of Ge-Si) also splits apart the energy sub-bands
  - Higher occupancy of lower m* band =>higher μ
- Operation of MOS devices at 500mV (or less) appears possible

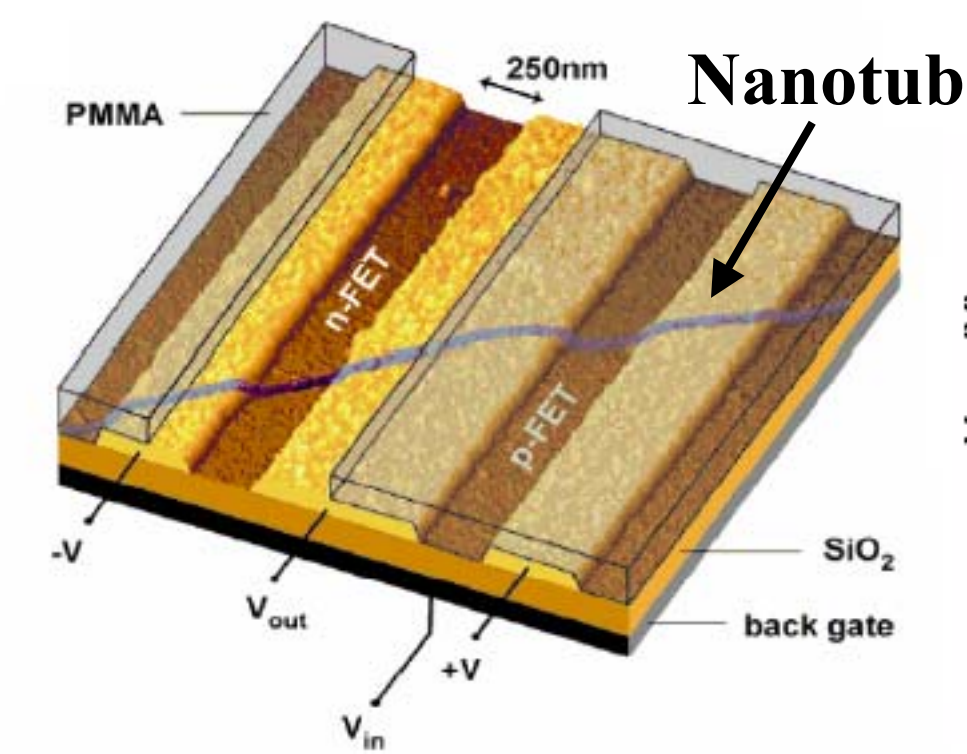
Agenda

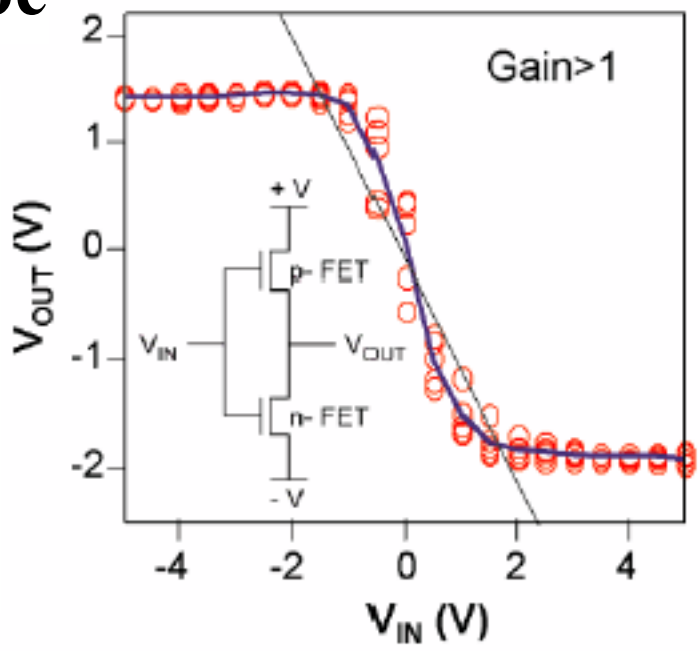
- Solid State Physics Refresher
- MOS Device Physics Refresher
- Classical CMOS Limitations
- Non-classical CMOS
- ***New Emerging Technologies***
- Conclusions

Emerging Technology Sequence



Nanotube FETs – CMOS Inverter

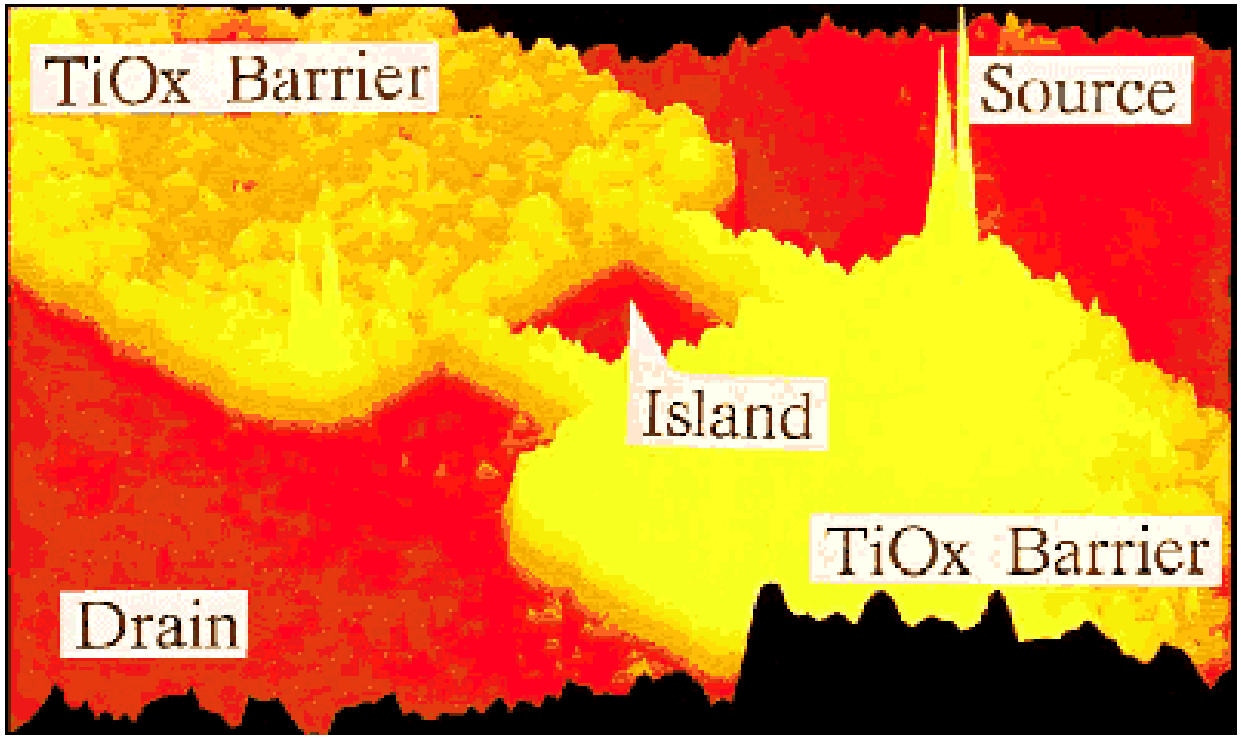




AFM image of logic gate

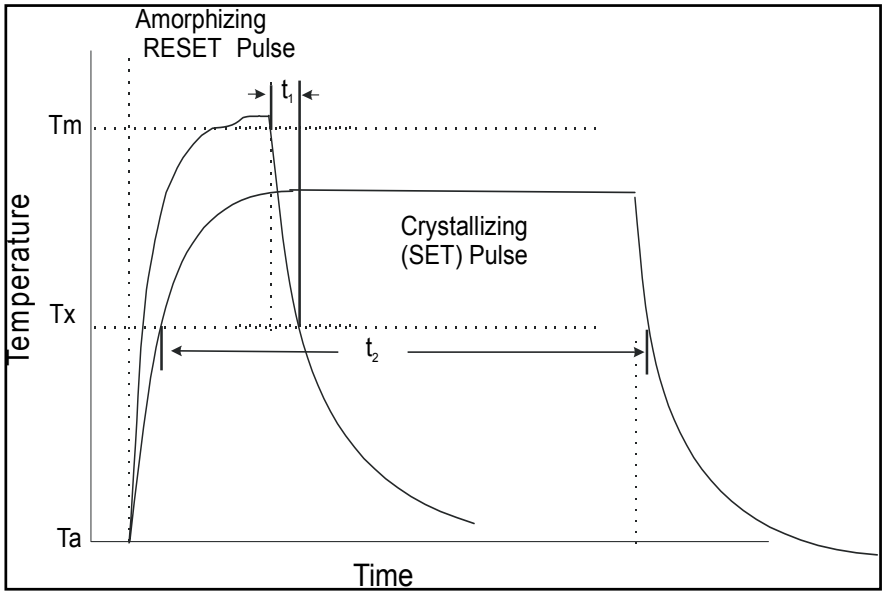
Room temperature Single Electron Transistor (SET)

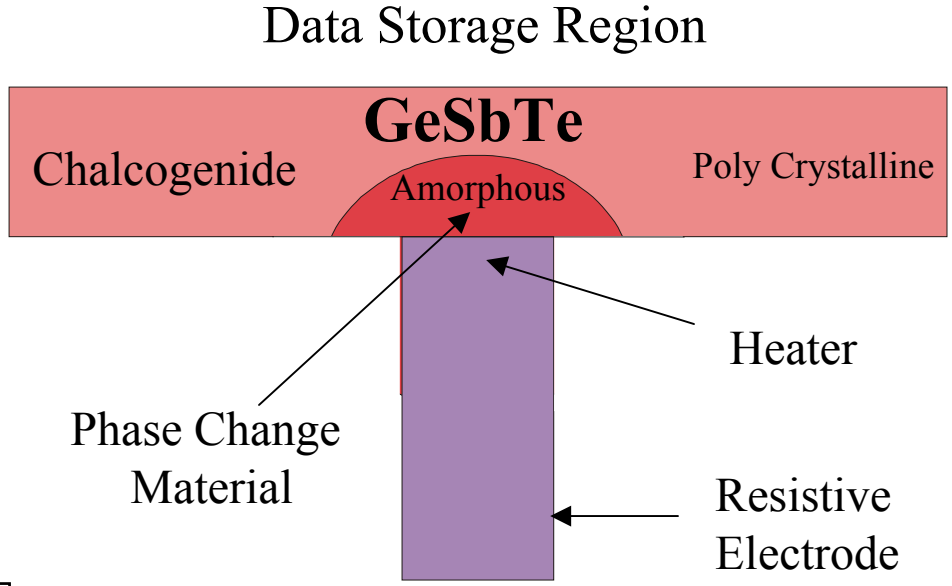
- Single electron in "island" controls current flow from source to drain
- Typical sizes of the TiOx lines are 15-25 nm widths and 30-50 nm lengths.
- Typical island sizes are 30-50 nm by 35-50 nm



What Is OUM?

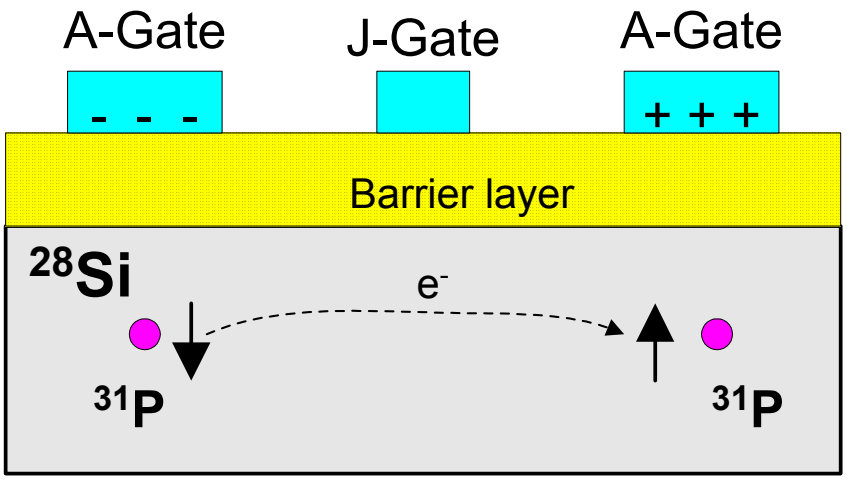
- **Operation**
  - **Chalcogenide material alloys used in re-writable CDs and DVDs**
  - **Electrical energy (heat) converts the material between crystalline (conductive) and amorphous (resistive) phases**
  - **Cell reads by measuring resistance**





- Attributes
  - + Non-volatile
  - + High density
  - + Non-destructive read
  - + Low voltage and low power
  - + ~10^{12} write/erase cycles
  - + Easy to integrate w/ logic

Quantum Computer

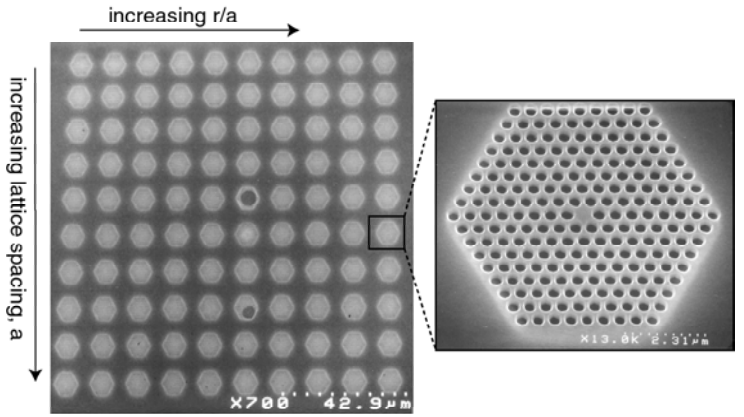


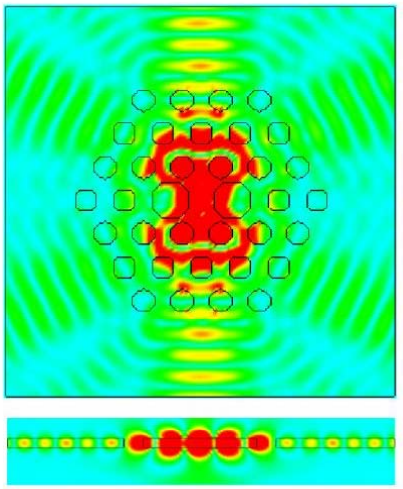
- Interactions between spin transistors can be controlled with gate structures
- Interaction is called "entanglement"
- Enables massively parallel operations
- Key applications include
  - Quantum cryptography
  - Factoring

Photonic devices

Man-made crystals produced by etching precisely placed holes in silicon or III-V material

Can produce, detect and manipulate light more efficiently than naturally occurring materials





Agenda

- Solid State Physics Refresher
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Conclusions

- **CMOS** will **remain** the main device technology of choice for the foreseeable future **(>10yrs)**
- Introduction of **Non-classical** CMOS in manufacturing will occur within this decade **(~5years)**
- Many **new materials** will be necessary
- **Band** engineering represents the next opportunity for **performance** improvement
- Economical engineering of the **starting wafer** material represents a major challenge for this industry
- 30 years of profitable investment in new equipment capabilities are making the evaluation of **nano-structures**, slated for practical **manufacturing 10 years** from now, possible today